

Course Description

Attending the *Designing a LogiCORE PCI Express System* will provide you a working knowledge of how to implement a Xilinx PCI Express® core in your applications. This course focuses on the implementation of a Xilinx PCI Express system with supporting logic and example designs. With this experience, you can improve your time to market with your PCIe core design. Various Xilinx PCI Express core products will be enumerated to aid you in selecting the proper solution. This course focuses on the Spartan®-6 PCIe endpoint and touches on the Virtex®-6 Root Complex.

Level – Intermediate

Course Duration – 2 days

Price – \$1200 or 12 Xilinx Training Credits

Course Part Number – PCIE28000-113-ILT

Who Should Attend?

- Hardware designers who want to create applications using Xilinx IP cores for PCI Express
- Software engineers who want to understand the deeper workings of the Xilinx LogiCORE PCI Express solution
- System architects who want to leverage key Xilinx advantages related to performance, latency, and bandwidth in PCI Express applications

Prerequisites

- Comprehensive understanding of the PCIe protocol (2 hour review included)
- Solid knowledge of Verilog or VHDL
- Solid experience with commonly used simulation tools such as Mentor Graphics ModelSim or ISIM
- Basic knowledge of Xilinx ISE® software
- *Designing for Performance and Designing with Multi-Gigabit Serial I/O* are recommended

Software Tools

- Xilinx ISE Design Suite: System Edition 11.3
- ISIM 11.3
- ChipScope Pro 11.3

After completing this comprehensive training, you will have the necessary skills to:

- Construct a basic PCIe system:
 - Select the appropriate core for your application
 - Specify and design an example endpoint application
 - Connect the PCIe core with the user endpoint functionality
 - Utilize FPGA resources to support the core
 - Simulate the design
- Identify the advanced capabilities of the PCIe specification protocol and feature set

Course Outline

Day 1

- Course Introduction
- Introduction to PCIe
- Review of the PCIe System Architecture and Protocol
- PCIe and CORE Generator
- **Lab 1:** Constructing the PCIe Core
- Simulating a PCIe Design
- Connecting Logic to the Core – Local Link
- Mem Read, Mem Write, Completion Packet details

- **Lab 2:** Downstream Port Model Simulation
- Endpoint Application Considerations
- **Lab 3:** Pseudo-Transactional Modeling

Day 2

- Typical application – DMA design review
- **Lab 4:** Implementing the Design
- Root Complex in Virtex-6
- Compliance and Debugging
- **Lab 5:** Debugging the PCIe Core with the ChipScope Pro Tools
- Errors and Interrupts
- Course Summary

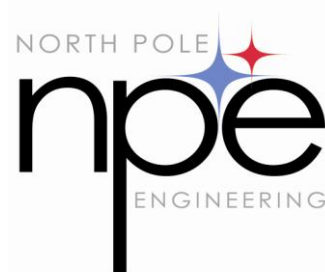
Lab Descriptions

- **Lab 1: Constructing the PCIe Core:** Familiarizes you with all the flow of the Xilinx CORE Generator™ software for generating a Xilinx LogiCORE™ PCIe core. You will select appropriate parameters for the CORE Generator tool and create the PCIe core used throughout the labs
- **Labs 2: Downstream Port Simulation:** Provides an overview of simulating the core using the ISim tool. You will observe and capture the effects of link training and write packets to the endpoint application.
- **Lab 3: Pseudo-Transactional Simulation:** Downstream Port Simulation is very time consuming. The solution to this is to run Pseudo-Transactional Simulation. This type of modeling enables the designer to test how the endpoint design will behave against various types of packets without having to simulate multiple PCIe cores.
- **Lab 4: Implementing the Design:** Familiarizes you with all the necessary steps and recommended settings to turn the HDL source to a bitstream.
- **Lab 5: Debugging Strategies:** Using a traffic simulator, you will use the ChipScope™ Pro tools to monitor the behavior of the core and the endpoint application for proper operation.

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