

Course Description

Xilinx FPGAs provide a new level of system design capabilities through soft MicroBlaze™ processors, hard PowerPC® processors, and silicon-efficient architectural resources. This course brings experienced FPGA designers up to speed on developing embedded systems using the Embedded Development Kit (EDK). The features and capabilities of the Xilinx MicroBlaze soft processor and the PowerPC 440 processor are also included in the lectures and labs. The hands-on labs provide experience with the development, debugging, and simulation of an embedded system.

Level – Intermediate

Course Duration – 2 days Xilinx

Price – \$1200 or 12 Xilinx Training Credits

Course Part Number – EMBD21000-10-ILT

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx MicroBlaze soft processor or IBM PowerPC 440 core using the Embedded Development Kit and a Xilinx FPGA

Prerequisites

- FPGA design experience
- Completion of the *Fundamentals of FPGA Design* course or equivalent knowledge of Xilinx ISE® software implementation tools
- Basic understanding of C programming
- Some HDL modeling experience

Software Tools

- Xilinx ISE® Foundation™ design tools 10.1 with the ISE Simulator
- Embedded Development Kit 10.1 with the Software Development Kit (SDK)
- Mentor Graphics ModelSim

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass the Xilinx Embedded Development Kit (EDK)
- Rapidly architect an embedded system containing a MicroBlaze or IBM PowerPC processor and Xilinx-supplied CoreConnect bus architecture IP by using the Base System Builder (BSB)
- Utilize the Eclipse-based Software Development Kit (SDK) to develop software applications and debug software
- Create and integrate your own IP into the EDK environment

Course Outline

Day 1

- EDK Overview
- Base System Builder
- **Lab 1:** Hardware Construction with the Base System Builder
- Software Development Using SDK
- **Lab 2:** Software, Implementation, and Download
- System Buses
- Hardware Design
- Hardware Design Using EDK
- **Lab 3:** Adding IP to a Hardware Design

Day 2

- Adding Your Own IP to the Embedded System
- **Lab 4:** Adding Custom IP to an Embedded System

- Software Debugging
- Linker Script Generator
- **Lab 5:** Software Debugging
- System Simulation
- **Lab 6:** Performing System Simulation

Lab Descriptions

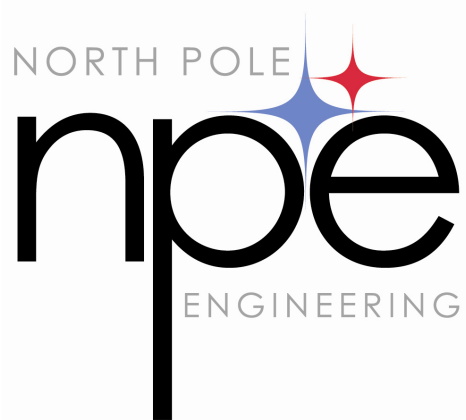
Both the MicroBlaze and PowerPC 440 processors are supported in the labs. All labs target the ML507 board.

- **Lab 1:** Hardware Construction with the Base System Builder – Create an XPS project by using the Base System Builder to develop a basic hardware system and generate a series of netlists for the embedded design.
- **Lab 2:** Software, Implementation, and Download – Complete the processes begun in Lab 1 by building the software libraries and applications, generating a bitstream file, merging the application into the bitstream, and downloading to the ML507 board.
- **Lab 3:** Adding IP to a Hardware Design – Learn to add IP from the many choices in the IP library. Use the GUI to add a general-purpose I/O module and access internal block RAM directly from the MHS file.
- **Lab 4:** Adding Custom IP to an Embedded System – Add custom IP to your design by using the Create and Import Peripheral wizard.
- **Lab 5:** Software Debugging – Run the Software Development Kit (SDK) to produce a debug perspective, set breakpoints, and debug the application.
- **Lab 6:** Performing System Simulation – Use ISIM to perform behavioral simulation of the completed design.

Register Today

NPE delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

Visit www.npe-inc.com/home/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard) as well as purchase orders and training credits.