Introduction to the AccelDSP Synthesis Tool

DSP12000-10-ILT (v1.0)

Course Specification

Course Description

Learn how to synthesize an algorithm written in the language of the MATLAB® software into a design that is optimized for a Xilinx FPGA. Find out how to make coding changes in the MATLAB software that improve area and performance. Use the floating-point to fixed-point and design exploration features of the AccelDSP™ synthesis tool to achieve maximum results. Merge a synthesized MATLAB software block into a larger HDL design or System Generator design.

Level – Fundamental
Course Duration – 2 days
Price – $1200 or 12 Xilinx Training Credits
Course Part Number – DSP12000-10-ILT
Who Should Attend? – Engineers seeking to develop the necessary skills for designing DSP systems using the Xilinx AccelDSP synthesis tool running with MATLAB software
Prerequisites

- Fundamental knowledge of the MATLAB software
- Basics of digital signal processing theory

Software Tools

- Xilinx ISE® Foundation™ 10.1 software with the ISE Simulator
- AccelDSP synthesis tool 10.1
- System Generator for DSP 10.1
- MATLAB R2007b

After completing this comprehensive training, you will have the necessary skills to:

- Transform a non-synthesizable MATLAB software algorithm into a design that can be synthesized by the AccelDSP synthesis tool
- Identify the concepts of quantization as well as specify, monitor, and control bit growth in a MATLAB software design
- Use AccelDSP synthesis tool directives and coding style changes to optimize a design for performance and efficiency
- Integrate an AccelDSP synthesis tool-generated design into a larger HDL design
- Generate and merge an AccelDSP synthesis tool design into a larger System Generator design

Course Outline

Day 1

- Introduction to the AccelDSP Synthesis Tool and Lab
- Synthesizable MATLAB Software Design and Lab
- Quantization and Lab
- Multirate Design and Lab
- Using AccelWare Reference Designs and Lab

Day 2

- Design Exploration and Lab
- Adding Hardware Control and Lab
- Coding for Hardware Performance and Lab
- Synthesizing Complex Numbers and Lab
- Interfacing to System Hardware and Lab
- System Generator Integration and Lab

Lab Descriptions

- **Lab 1: Getting Started with the AccelDSP Synthesis Tool** – Learn the basic design flow through the AccelDSP synthesis tool.
- **Lab 2: Synthesizable MATLAB Software Design** – Modify a non-synthesizable MATLAB software design so that it can be synthesized by the AccelDSP synthesis tool.
- **Lab 3: Quantization** – Specify, monitor, and control bit growth in the synthesized design.
- **Lab 4: Multirate Design** – Set up the design to model the effects of decimation by 2. Create a synthesizable polyphase decimation filter in the MATLAB software and implement the filter in a Xilinx FPGA.
- **Lab 5: Using AccelWare Reference Designs** – Replace a polyphase decimation filter with an equivalent FIRdecim AccelWare™ reference design block.
- **Lab 6: Design Exploration** – Apply the design exploration features of the AccelDSP synthesis tool to optimize a design for area and performance.
- **Lab 7: Adding Hardware Control** – Modify the source of a FIR filter to add a serial coefficients load feature.
- **Lab 8: Coding for Hardware Performance** – Learn coding techniques to take advantage of even-symmetric coefficients and drive higher performance.
- **Lab 9: Synthesizing Complex Numbers** – Explore the methods available for synthesizing designs that use complex numbers.
- **Lab 10: Interfacing to System Hardware** – Connect the interface signals generated in the AccelDSP synthesis tool to a larger HDL design.
- **Lab 11: System Generator Integration** – Convert a MATLAB software-based design into a System Generator block and merge the block into a larger System Generator design.

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