Vivado Design Suite for ISE Software Project Navigator Users

FPGA 2

VIVA10000-ILT (v1.0)

Course Specification

Course Description

This course offers introductory training on the Vivado® Design Suite. This course is for experienced ISE® software users who want to take full advantage of the Vivado Design Suite feature set. Learn about the Vivado Design Suite projects, design flow, Xilinx Design Constraints, and basic timing reports.

Level – FPGA 2

Course Duration – 1 day

Price – $700 or 7 Xilinx Training Credits

Course Part Number – VIVA10000-ILT

Who Should Attend? – Existing Xilinx ISE software Project Navigator FPGA designers

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design, Designing for Performance*, or *Advanced FPGA Implementation* courses or equivalent knowledge of the Xilinx ISE software implementation tools and device architecture
- Intermediate VHDL or Verilog knowledge

Recommended

- *Essential Tcl Scripting for the Vivado Design Suite* course

Software Tools

- Vivado Design or System Edition 2014.3

Hardware

- Architecture: 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board*

* This course focuses on the 7 series architecture. Check with North Pole Engineering, Inc., for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the Project Manager to start a new project
- Identify the available Vivado IDE design flows (project based and non-project batch)
- Identify file sets (HDL, XDC, simulation)
- Analyze designs using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize and implement an HDL design
- Utilize a systematic approach to apply timing constraints and achieve timing closure
- Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
- Use the primary Tcl-based reports (`check_timing`, `report_clock_interaction`, `report_clock_networks`, and `report_timing_summary`)

Course Outline

- UltraFast Design Methodology Summary
- Introduction to the Vivado Design Suite
- Vivado Design Flows
- **Lab 1:** Vivado Tool Overview
- Demo: Visualization for Design Analysis
- Designing with IP
- Demo: IP flow
- Demo: Designing with IPI
- Basic Timing Constraints and Reports
- **Lab 2:** Vivado Synthesis, Implementation, and Timing Closure
- Appendix: Visualization for Analysis
- Appendix: Designing with IP
- Appendix: Using the Pin Planning Environment

Lab Descriptions

- **Lab 1:** Vivado Tool Overview – Create a project in the Vivado Design Suite. Add files, simulate, and elaborate the design. Review the available reports, analyze the design with the Schematic and Hierarchy viewers, and run a design rule check (DRC). Finally, assign some of the I/O pins using the IO Planner.
- **Lab 2:** Vivado Synthesis, Implementation, and Timing Closure – Synthesize and analyze the design with the Schematic viewer. Utilize a systematic approach to apply timing constraints and achieve timing closure(i.e., understand the Xilinx baselining recommendation). Run basic static timing analysis using the `check_timing` and `report_clock_utilization` reports. Implement the design and analyze some timing-critical paths with the Schematic viewer. Download the bitstream to the demonstration board.

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