

### Course Description

Learn how to use basic Tcl syntax and language structures to build scripts suitable for use with Xilinx FPGA design tools. Learn about the effective use of variables, data types, and Tcl constructs to build effective conditional statements and loop controls. You will also have the opportunity to use Tcl language constructs with several labs designed to provide you scripting experience within the Vivado® Design Suite.

**Level** – FPGA 1

**Course Duration** – 1 day

**Price** – \$700 or 7 Xilinx Training Credits

**Course Part Number** – LANG13000-ILT

**Who Should Attend?** – FPGA designers and logic designers

#### Prerequisites

- FPGA design experience or completion of the *Essentials of FPGA Design* course

#### Software Tools

- Vivado Design or System Edition 2014.3

#### Hardware

- Architecture: N/A\*
- Demo board: None\*

\* This course does not focus on any particular architecture. Check with North Pole Engineering, inc., for specifics or other customizations. After completing this comprehensive training, you will have the necessary skills to:

- Describe the basic syntax and language structure of the Tcl language
- Execute Tcl commands from a script using the Vivado IDE
- Use the Xilinx Tcl Store
- Use variables and describe data types
- Use Tcl language constructs to build conditional statements and loop controls for some common FPGA applications
- Use lists and arrays in efficient data structures
- Use procedures, packages, and namespaces to develop modules

### Course Outline

- Introduction to the Tcl Environment
- **Lab 1:** Introduction to the Vivado IDE Tcl Environment
- Using Tcl in the Vivado IDE
- Demo: Tcl Project-Based Flow
- Introduction to the Xilinx Tcl Store
- Demo: Using the Xilinx Tcl Store
- **Lab 2:** Xilinx Tcl Scripting
- Basic Syntax and Structure
- Data Types, Variables, and Expressions
- Conditional Expressions and Loops
- **Lab 3:** Manipulating Pin Attributes with Tcl
- Lists
- Data Structures and Xilinx-Specific Tcl commands
- **Lab 4:** Design Analysis with the Vivado IDE
- Procedures and Packages
- Tcl Regular Expressions
- **Lab 5:** Using Regular Expressions

- Appendix: Debugging and Error Management
- Appendix: Regular Tcl Expressions

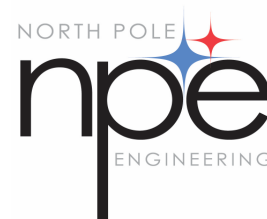
### Lab Descriptions

- **Lab 1:** Introduction to the Vivado IDE Tcl Environment – Learn some basic ways of interfacing with the operating system and explore commonly used Tcl commands.
- **Lab 2:** Basic Tcl Scripting – Learn how to use Tcl scripts in a typical FPGA design flow using the Vivado IDE.
- **Lab 3:** Manipulating Pin Attributes with Tcl – Learn to query your design netlist and verify the use of various Tcl commands with the Vivado IDE. You will also learn to make pin assignments and verify resource usage with appropriate Vivado IDE reports.
- **Lab 4:** Design Analysis with the Vivado IDE – This lab introduces some of the most important reporting and design analysis features provided by the Vivado Design Suite. In this lab, you will use Tcl commands to query the design netlist and locate clock sources. You will also use the `check_timing` and `report_timing` commands to verify design performance.
- **Lab 5:** Using Regular Expressions – Query timing reports to find critical timing information and build a custom timing report while using file I/O commands and regular expressions to extract essential information with a script.

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