Designing with SystemVerilog

FPGA 1

LANG-SVDES-ILT (v1.0)

Course Specification

Course Description

This comprehensive course is a thorough introduction to SystemVerilog constructs for design. This class addresses writing RTL code using the new constructs available in SystemVerilog. New data types, structs, unions, arrays, procedural blocks, re-usable tasks, functions, and packages are all covered. The information gained can be applied to any digital design. This course combines insightful lectures with practical lab exercises to reinforce key concepts.

In this two-day course, you will gain valuable hands-on experience. Incoming students with a Verilog background will finish this course empowered with the ability to more efficiently develop RTL designs.

Level – FPGA 1

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – LANG-SVDES-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog design experience or completion of Designing with Verilog

Software Tools

- Vivado® Design or System Edition 2017.1
- Questa Sim Prime Simulator 10.5b

Hardware

- Architecture: N/A*
- Demo board: Kintex® UltraScale™ FPGA KCU105 or Kintex-7 FPGA KC705 board*

* This course does not focus on any particular architecture. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the features and benefits of using SystemVerilog for RTL design
- Identify the new data types supported in SystemVerilog
- Use an enumerated data type for coding a finite state machine (FSM)
- Explain how to use structures, unions, and arrays
- Describe the new procedural blocks and analyze the affected synthesis results
- Define the enhancements and ability to reuse tasks, functions, and packages
- Identify how to simplify module definitions and instantiations using interfaces
- Examine how to efficiently code in SystemVerilog for FPGA design simulation and synthesis
- Target and optimize Xilinx FPGAs by using SystemVerilog
- Synthesize and analyze SystemVerilog designs with the Vivado Design Suite
- Download a complete SystemVerilog design to an evaluation board

Course Outline

Day 1

- Introduction to SystemVerilog
- Data Types
- Demo: SystemVerilog Integer Data Types
- **Lab 1:** SystemVerilog Data Types
- Structures, Unions, and Arrays
- **Lab 2**: Structures and Unions
- Additional Operators in SystemVerilog
- Procedural Statements and Flow Control
- **Lab 3:** always_ff and always_comb Procedural Blocks

Day 2

- Functions, Tasks, and Packages
- **Lab 4**: Functions, Tasks, and Packages
- Interfaces
- Targeting Xilinx FPGAs
- **Lab 5:** Interfaces and Design Download

Lab Descriptions

- **Lab 1:** SystemVerilog Data Types – Use enumerated data types to build a finite state machine and perform synthesis to analyze the results.
- **Lab 2:** Structures and Unions - Learn about packed and unpacked structures and unions and how to access their members.
- **Lab 3:** always_ff and always_comb Procedural Blocks – Learn to use the new procedural blocks always_comb, always_ff, and always_latch to produce the intended synthesized results.
- **Lab 4:** Functions, Tasks, and Packages - Create a new package and import that package into the module.
- **Lab 5:** Interfaces and Design Download – Use an interface to simplify the module inputs and outputs. Download and verify the design in-circuit.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

Visit **www.npe-inc.com/training**, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.