

Course Description

This course teaches hardware designers who are new to high-speed memory I/O to design a memory interface in Xilinx FPGAs. It introduces designers to the basic concepts of high-speed memory I/O design, implementation, and debugging using Spartan®-6 and Virtex®-6 FPGAs. Additionally, you will learn about the tools available for high-speed memory interface design, implementation, and debugging.

The major memory types covered are DDR, DDR2, DDR3, RLDRAMII, LPDDR, QDRII, and QDRII+. Labs are available for DDR2 on the SP601, DDR3 on the ML605, or DDR3 on the SP605 demo board.

Level – Connectivity 3

Course Duration – 2 days

Price – \$1200 or 12 Xilinx Training Credits

Course Part Number – MEM21000-13-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- VHDL or Verilog experience or *Designing with VHDL* or *Designing with Verilog* course
- Familiarity with logic design: state machines and synchronous design
- Very helpful to have:
 - Basic knowledge of FPGA architecture
 - Familiarity with Xilinx implementation tools
- Nice to have:
 - Familiarity with I/O basics
 - Familiarity with high-speed I/O standards

Software Tools

- Xilinx ISE® Design Suite: Logic or System Edition 13.1
- Mentor HyperLynx SI

Hardware

- Architecture: Spartan®-6 and Virtex®-6 FPGAs*
- Demo board: Spartan-6 FPGA SP601/SP605 or Virtex-6 FPGA ML605 board*

* This course focuses on the Spartan-6 and Virtex-6 architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Identify the FPGA resources required for memory interfaces
- Describe different types of memories
- Utilize the Xilinx tools to generate memory interface designs
- Simulate memory interfaces with the Xilinx ISim simulator
- Implement memory interfaces
- Identify the board design options for the realization of memory interfaces
- Describe PCB-level simulation
- Test and debug your memory interface design

Course Outline

Day 1

- Introduction
- Spartan-6 and Virtex-6 Family Overview
- Memory Devices
- Spartan-6 FPGA Memory Interfaces
- Virtex-6 FPGA Memory Interfaces

- MIG Design Generation
- **Lab 1:** MIG Core Generation

Day 2

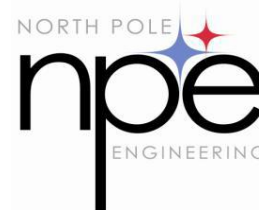
- MIG Design Simulation
- **Lab 2:** MIG Design Simulation
- MIG Design Implementation
- **Lab 3:** MIG Design Implementation
- Memory Interface Board-Level Design
- Memory Interface PCB Simulation
- **Lab 4:** Signal Integrity Simulation
- Memory Interface Test and Debugging
- **Lab 5:** MIG Design Debugging

Lab Descriptions

- **Lab 1:** MIG Core Generation – Create a DDR2 or DDR3 memory controller using the Memory Interface Generator (MIG) CORE Generator™ interface. For Spartan-6 devices, customize the hard Memory Controller Block (MCB) targeting the SP601 or SP605 board. For Virtex-6 devices, customize the soft core memory controller for the ML605 board.
- **Lab 2:** MIG Design Simulation – Simulate the memory controller created in Lab 1 using ISim.
- **Lab 3:** MIG Design Implementation – Implement the memory controller created in the previous labs. Modify constraints, synthesize, implement, create the bitstream, program the FPGA, and check the functionality.
- **Lab 4:** Signal Integrity Simulation – Evaluate and perform basic verification options available for IBIS simulation of memory interfaces.
- **Lab 5:** MIG Design Debugging – Debug the memory interface design utilizing the ChipScope Pro™ tool.

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