Designing FPGAs Using the Vivado Design Suite 4

FPGA 4

FPGA-VDES4-ILT (v1.0)

Course Specification

Course Description

This course tackles the most sophisticated aspects of the Vivado® Design Suite and Xilinx hardware. This course enables you to use the advanced capabilities of the Vivado Design Suite to achieve design closure.

Level – FPGA 4

Course Duration – 2 days

Price – $1400 or 14 Xilinx Training Credits

Course Part Number – FPGA-VDES4-ILT

Who Should Attend? – Engineers who seek advanced training in using Xilinx tools to improve FPGA performance and utilization while also increasing productivity

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 2* course
- *Designing FPGAs Using the Vivado Design Suite 3* course
- At least six months of design experience with Xilinx tools and FPGAs

Software Tools

- Vivado Design or System Edition 2016.3

Hardware

- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board

* This course focuses on the UltraScale and 7 series architectures. Check with your local Authorized Training Provider for specifics or other customizations. The number of topic modules provided is greater than can be covered in two days. The instructor will select modules covered in class. Check with North Pole Engineering, Inc., for the specifics of in-class lab board and other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Apply appropriate I/O timing constraints and design modifications for source-synchronous and system-synchronous interfaces
- Analyze a timing report to identify how to center the clock in the data eye
- Use Tcl scripting in non-project batch flows to synthesize, implement, and generate custom timing reports
- Utilize floorplanning techniques to improve design performance
- Employ advanced implementation options, such as incremental compile flow, physical optimization techniques, and re-entrant mode as last mile strategies
- Utilize Xilinx security features, bitstream encryption, and authentication using AES for design and IP security
- Identify advanced FPGA configurations, such as daisy chains and gangs, for configuring multiple FPGAs in a design
- Debug a design at the device startup phase to debug issues related to startup events, such as MMCM lock and design coming out of reset

Course Outline

Day 1

- UltraFast Design Methodology Introduction {Lecture}
- Scripting in Vivado Design Suite Non-Project Mode {Lecture, Lab}
- Using Procedures and Lists in Tcl Scripting {Lecture}
- Using regexp in Tcl Scripting {Lecture, Lab}
- Introduction to the Xilinx Tcl Store {Lecture, Demo}
- Debugging and Error Management in Tcl Scripting {Lecture}
- I/O Timing Scenarios {Lecture}
- Source-Synchronous I/O Timing {Lecture, Lab}
- System-Synchronous I/O Timing {Lecture, Demo}
- Timing Constraints Priority {Lecture}
- Case Analysis {Lecture}
- Daisy Chains and Gangs in Configuration {Lecture}
- Managing Remote IP {Lecture, Lab}

Day 2

- Introduction to Floorplanning {Lecture}
- Design Analysis and Floorplanning {Lecture, Lab}
- Incremental Compile Flow {Lecture, Lab}
- Physical Optimization {Lecture, Lab}
- Vivado Design Suite ECO Flow {Lecture, Lab}
- Trigger and Debug at Device Startup {Lecture, Demo}
- Scripting for a VLA Design {Lecture, Lab}
- Vivado Design Suite Debug Methodology {Lecture}
- Power Management Techniques {Lecture}
- Bitstream Security {Lecture, Lab}

Topic Descriptions

Day 1

- UltraFast Design Methodology Introduction – Introduces the UltraFast™ design methodology guidelines covered in this course.
- Scripting in Vivado Design Suite Non-Project Mode – Write Tcl commands in the non-project batch flow for a design.
- Using Procedures and Lists in Tcl Scripting – Employ procedures and lists in Tcl scripting.
- Using regexp in Tcl Scripting – Use regular expressions to find a pattern in a text file while scripting an action in the Vivado Design Suite.
- Introduction to the Xilinx Tcl Store – Introduces the Xilinx Tcl Store.
- Debugging and Error Management in Tcl Scripting – Understand how to debug errors in a Tcl script.
- I/O Timing Scenarios – Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.
- Source-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.
- System-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.
- Timing Constraints Priority – Identify the priority of timing constraints.
- Case Analysis – Understand how to analyze timing when using multiplexed clocks in a design.
- Daisy Chains and Gangs in Configuration – Introduces advanced configuration schemes for multiple FPGAs.
- Managing Remote IP – Store IP and related files remote to the current working project directory.

Day 2

- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Design Analysis and Floorplanning – Explore the pre- and post-implementation design analysis features of the Vivado IDE.
- Incremental Compile Flow – Utilize the incremental compile flow when making last-minute RTL changes.
- Physical Optimization – Use physical optimization techniques for timing closure.
- Vivado Design Suite ECO Flow – Use ECO flow to make changes to a previously implemented design and apply changes to the original design.

- Trigger and Debug at Device Startup – Debug the events around the device startup.
- Scripting for a VLA Design – Use Tcl scripting for VLA designs for adding probes and making connections to probes.
- Vivado Design Suite Debug Methodology – Understand and follow the debug core recommendations. Employ the debug methodology for debugging a design using the Vivado logic analyzer.
- Power Management Techniques – Identify techniques used for low power design.
- Bitstream Security – Understand the Xilinx bitstream security features such as readback disable, bitstream encryption, and authentication.

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- Student cancellations must be sent here.

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