Designing FPGAs Using the Vivado Design Suite 3

FPGA 3

FPGA-VDES3-ILT (v1.0)

Course Specification

Course Description

This course demonstrates timing closure techniques, such as baselining, pipelining, synchronization circuits, and optimum HDL coding techniques that help with design timing closure. This course also shows you how to debug your design using advanced capabilities of the Vivado® logic analyzer.

Level – FPGA 3

Course Duration – 2 days

Price – $1400 or 14 Xilinx Training Credits

Course Part Number – FPGA-VDES3-ILT

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and FPGA architecture and some experience with the Vivado Design Suite

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- *Designing FPGAs Using the Vivado Design Suite 2* course
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Optional Videos

- Basic HDL Coding Techniques*
- Power Estimation*

Software Tools

- Vivado Design or System Edition 2016.3

Hardware

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board: Kintex®-7 FPGA KC705 board

* Go to www.xilinx.com/training and click the Online Training tab to view these videos.

** This course focuses on the UltraScale and 7 series architectures. The number of topic modules provided is greater than can be covered in two days. The instructor will select modules covered in class. Check with North Pole Engineering, Inc., for the specifics of in-class lab board and other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Employ good alternative design practices to improve design reliability
- Define a properly constrained design
- Apply baseline constraints to determine if internal timing paths meet design timing objectives
- Optimize HDL code to maximize the FPGA resources that are inferred and meet performance goals
- Build a more reliable design that is less vulnerable to metastability problems and requires less design debugging later in the development cycle
- Increase performance by utilizing FPGA design techniques
- Use Vivado Design Suite reports and utilities to full advantage, especially the Clock Interaction report

Course Outline

Day 1

- UltraFast Design Methodology Introduction {Lecture}
- Timing Simulation {Lecture, Lab}
- Vivado Design Suite Non-Project Mode {Lecture}
- Revision Control Systems in the Vivado Design Suite {Lecture, Lab}
- Baselining {Lecture, Lab, Demo}
- Pipelining {Lecture, Lab}
- Inference {Lecture, Lab}
- Report Clock Interaction {Lecture, Demo}

Day 2

- Synchronization Circuits {Lecture, Demo}
- Report Datasheet {Lecture, Demo}
- Configuration Modes {Lecture}
- Dynamic Power Estimation Using Vivado Report Power {Lecture, Lab}
- Debug Flow in an IP Integrator Block Design {Lecture, Lab}
- Remote Debugging Using the Vivado Logic Analyzer {Lecture, Lab}
- JTAG to AXI Master Core {Lecture, Demo}
- Trigger Using the Trigger State Machine in the Vivado Logic Analyzer {Lecture, Lab}
- Manipulating Design Properties Using Tcl {Lecture, Lab}

Topic Descriptions

Day 1

- UltraFast Design Methodology Introduction – Introduces the methodology guidelines covered in this course.
- Timing Simulation – Simulate the design post-implementation to verify that a design works properly on hardware.
- Vivado Design Suite Non-Project Mode – Create a design in the Vivado Design Suite non-project mode.
- Revision Control Systems in the Vivado Design Suite – Use version control systems with Vivado design flows.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Pipelining – Use pipelining to improve design performance.
- Inference – Infer Xilinx dedicated hardware resources by writing appropriate HDL code.
- Report Clock Interaction – Use the clock interaction report to identify interactions between clock domains.

Day 2

- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Report Datasheet – Use the datasheet report to find the optimal setup and hold margin for an I/O interface.
- Configuration Modes – Understand various configuration modes and select the suitable mode for a design.
- Dynamic Power Estimation Using Vivado Report Power – Use an SAIF (switching activity interface format) file to determine accurate power consumption for a design.
- Debug Flow in an IP Integrator Block Design – Insert the debug cores into IP integrator block designs.
- Remote Debugging Using the Vivado Logic Analyzer – Use the Vivado logic analyzer to configure an FPGA, set up triggering, and view the sampled data from a remote location.
- JTAG to AXI Master Core – Use this debug core to write/read data to/from a peripheral connected to an AXI interface in a system that is running in hardware.
- Trigger Using the Trigger State Machine in the Vivado Logic Analyzer – Use trigger state machine code to trigger the ILA and capture data in the Vivado logic analyzer.
- Manipulating Design Properties Using Tcl – Query your design and make pin assignments by using various Tcl commands.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

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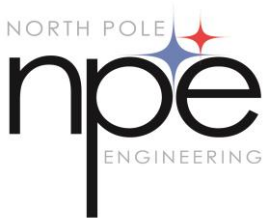

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

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- Student cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

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- We regret from time to time classes will need to be rescheduled or cancelled.
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- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- For additional information or to schedule a private class contact us here.