Designing FPGAs Using the Vivado Design Suite 2

FPGA 2

FPGA-VDES2-ILT (v1.0)

Course Specification

Course Description

This course shows you how to to build an effective FPGA design using synchronous design techniques, using the Vivado® IP integrator to create a sub-system, using proper HDL coding techniques to improve design performance, and debugging a design with multiple clock domains.

Level – FPGA 2

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – FPGA-VDES2-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and who are new to Xilinx FPGAs

Prerequisites

- Designing FPGAs Using the Vivado Design Suite 1 course
- Working HDL knowledge (VHDL or Verilog)
- Digital design experience

Software Tools

- Vivado Design or System Edition 2017.1

Hardware

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board (optional): Kintex®-7 FPGA KC705 board**

** This course focuses on the UltraScale and 7 series architectures. Check with North Pole Engineering, Inc., for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Create a Tcl script to create a project, add sources, and implement a design
- Describe and use the clock resources in a design
- Build resets into your system for optimum reliability and design speed
- Apply timing exception constraints in a design as part of the Baselining procedure to fine tune the design
- Use the Vivado IP integrator to create a block design
- Create and package your own IP and add to the Vivado IP catalog to reuse
- Describe the HLx design flow that increase productivity
- Debug a design with multiple clock domains with the help of multiple debug cores using the Vivado logic analyzer
- Identify synchronous design techniques
- Describe how an FPGA is configured

Course Outline

This course has more material than can be covered in two days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student interest.

Day 1

- UltraFast Design Methodology: Design Creation and Analysis {Lecture}
- Synchronous Design Techniques {Lecture}
- Resets {Lecture, Lab}
- Register Duplication {Lecture}
- Scripting in Vivado Design Suite Project Mode {Lecture, Lab}
- Clocking Resources {Lectures, Lab}
- I/O Logic Resources {Lectures}
- Creating and Packaging Custom IP {Lecture, Lab}
- Using an IP Container {Lecture, Demo}
- Designing with IP Integrator {Lecture, Lab, Demo, Case Study}

Day 2

- Timing Summary Report {Lecture, Demo}
- Generated Clocks {Lecture, Demo}
- Clock Group Constraints {Lecture, Demo}
- Introduction to Timing Exceptions {Lecture, Lab, Demo}
- Power Analysis and Optimization Using the Vivado Design Suite {Lecture, Lab}
- Introduction to the HLx Design Flow {Lecture, Lab, Demo}
- Configuration Process {Lecture}
- Sampling and Capturing Data in Multiple Clock Domains {Lecture, Lab}
- Design Analysis Using Tcl Commands {Lecture, Demo, Lab}

Topic Descriptions

Day 1

- UltraFast Design Methodology: Design Creation and Analysis – Overview of the methodology guidelines covered in this course.
- Synchronous Design Techniques – Introduces synchronous design techniques used in an FPGA design.
- Resets – Investigates the impact of using asynchronous resets in a design.
- Register Duplication – Use register duplication to reduce high fanout nets in a design.
- Scripting in Vivado Design Suite Project Mode – Explains how to write Tcl commands in the project-based flow for a design.
- Clocking Resources – Describes various clock resources, clocking layout, and routing in a design.
- I/O Logic Resources – Overview of I/O resources and the IOB property for timing closure.
- Creating and Packaging Custom IP – Create your own IP and package and include it in the Vivado IP catalog.
- Using an IP Container – Use a core container file as a single file representation for an IP.
- Designing with IP Integrator – Use the Vivado IP integrator to create the uart_led subsystem.

Day 2

- Timing Summary Report – Use the post-implementation timing summary report to sign-off criteria for timing closure.
- Generated Clocks – Use the report clock networks report to determine if there are any generated clocks in a design.
- Clock Group Constraints – Apply clock group constraints for asynchronous clock domains.
- Introduction to Timing Exceptions – Introduces timing exception constraints and applying them to fine tune design timing.
- Power Analysis and Optimization Using the Vivado Design Suite – Use report power commands to estimate power consumption.
- Introduction to the HLx Design Flow – Use the HLx design flow to increase productivity and reduce run time when designing and verifying a design.
- Configuration Process – Understand the FPGA configuration process, such as device power up, CRC check, etc.
- Sampling and Capturing Data in Multiple Clock Domains – Overview of debugging a design with multiple clock domains that require multiple ILAs.
- Design Analysis Using Tcl Commands – Analyze a design using Tcl commands.

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