

### Course Description

This course offers introductory training on the Vivado® Design Suite and helps you to understand the FPGA design flow.

For those uninitiated to FPGA design, this course helps in designing an FPGA design, which includes creating a Vivado Design Suite project with source files, simulating the design, performing pin assignments, applying basic timing constraints, synthesizing, implementing, and debugging the design. Finally, the process for generating and downloading bitstream on a demo board is also covered.

#### Level – FPGA 1

**Course Duration** – 2 days

**Price** – \$1600 or 16 Xilinx Training Credits

**Course Part Number** – FPGA-VDES1-ILT

**Who Should Attend?** – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the Vivado Design Suite

#### Prerequisites

- Basic knowledge of the [VHDL](#) or [Verilog](#) language
- Digital design knowledge

#### Recommended pre-study

- Basic FPGA Architecture (7-Series):
  - [Slice and I/O Resources](#)
  - [Memory](#)
  - [Clocking Resources](#)
- Basic FPGA Architecture:
  - [Configurable Logic Block](#)
  - [Memory](#)
  - [Clocking resources](#)

#### Software Tools

- Vivado Design or System Edition 2017.1

#### Hardware

- Architecture: UltraScale™ and 7 series FPGAs\*\*
- Demo board (optional): Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board\*\*

\*\* This course focuses on the UltraScale and 7 series architectures. Check with [North Pole Engineering, Inc.](#) for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the New Project Wizard to create a new Vivado IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Synthesize and implement the HDL design
- Apply clock and I/O timing constraints and perform timing analysis
- Describe the "baselining" process to gain timing closure on a design
- Use the Schematic and Hierarchy viewers to analyze and cross-probe a design
- Use the Vivado logic analyzer and debug flows to debug a design

### Course Outline

This course has more material than can be covered in two days. All slides and lab instructions will be provided to students. Some instructors may present material out of sequence, offer custom presentations demonstrations and labs based on student consensus.

#### Day 1

- Introduction to FPGA Architecture, 3D IC, SoC {Lecture}

- UltraFast Design Methodology: Planning {Lecture, Demo}
- HDL Coding Techniques {Lecture}
- Introduction to Vivado Design Flows {Lecture}
- Vivado Design Suite Project Mode {Lectures, Lab}
- Synthesis and Implementation {Lecture, Lab}
- Basic Design Analysis in the Vivado IDE {Lab, Demo}
- Vivado Design Rule Checks {Lab}
- Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- Vivado IP Flow {Lecture, Lab, Demo}
- Timing Constraints Wizard {Lecture, Lab}
- Timing Constraints Editor {Lecture}
- Introduction to Vivado Reports {Lecture, Demo}

#### Day 2

- Introduction to Clock Constraints {Lecture, Lab, Demo}
- I/O Constraints and Virtual Clocks {Lecture, Lab}
- Setup and Hold Timing Analysis {Lecture}
- Report Clock Networks {Lecture, Demo}
- Xilinx Power Estimator Spreadsheet {Lecture, Lab}
- Introduction to FPGA Configuration {Lecture}
- Introduction to the Vivado Logic Analyzer {Lecture, Demo}
- Introduction to Triggering {Lecture}
- Debug Cores {Lecture}
- HDL Instantiation Debug Probing Flow {Lecture, Lab}
- Netlist Insertion Debug Probing Flow {Lecture, Lab}
- Introduction to the Tcl Environment {Lecture, Lab}
- Using Tcl Commands in the Vivado Design Suite Project Flow {Lecture, Demo}
- Tcl Syntax and Structure {Lecture}

### Topic Descriptions

#### Day 1

- Introduction to FPGA Architecture, 3D IC, SoC – Overview of FPGA architecture, SSI technology, and SoC device architecture.
- UltraFast Design Methodology: Planning – Introduces the methodology guidelines covered in this course and the UltraFast Design Methodology checklist.
- HDL Coding Techniques – Covers basic digital coding guidelines used in an FPGA design.
- Introduction to Vivado Design Flows – Introduces the Vivado design flows: the project flow and non-project batch flow.
- Vivado Design Suite Project Mode – Create a project, add files to the project, explore the Vivado IDE, and simulate the design.
- Synthesis and Implementation – Create timing constraints according to the design scenario and synthesize and implement the design. Optionally, generate and download the bitstream to the demo board.
- Basic Design Analysis in the Vivado IDE – Use the various design analysis features in the Vivado Design Suite.
- Vivado Design Rule Checks – Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations.
- Vivado Design Suite I/O Pin Planning – Use the I/O Pin Planning layout to perform pin assignments in a design.
- Vivado IP Flow – Customize IP, instantiate IP, and verify the hierarchy of your design IP.
- Timing Constraints Wizard – Use the Timing Constraints Wizard to apply missing timing constraints in a design.

**FPGA-VDES1-ILT (v1.0)****Course Specification**

- Timing Constraints Editor – Introduces the timing constraints editor tool to create timing constraints.
- Introduction to Vivado Reports – Generate and use Vivado timing reports to analyze failed timing paths.

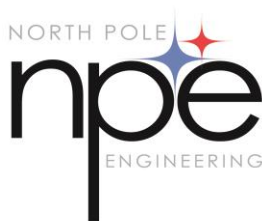
**Day 2**

- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.
- I/O Constraints and Virtual Clocks – Apply I/O constraints and perform timing analysis.
- Setup and Hold Timing Analysis – Understand setup and hold timing analysis.
- Report Clock Networks – Use `report clock networks` to view the primary and generated clocks in a design.
- Xilinx Power Estimator Spreadsheet – Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.
- Introduction to FPGA Configuration – Describes how FPGAs can be configured.
- Introduction to the Vivado Logic Analyzer – Overview of the Vivado logic analyzer for debugging a design.
- Introduction to Triggering – Introduces the trigger capabilities of the Vivado logic analyzer.
- Debug Cores – Understand how the debug hub core is used to connect debug cores in a design.
- HDL Instantiation Debug Probing Flow – Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- Netlist Insertion Debug Probing Flow – Use the Netlist Insertion flow to insert ILA cores into an existing synthesized netlist and debug a common problem.
- Introduction to the Tcl Environment – Introduces Tcl (tool command language).
- Using Tcl Commands in a Vivado Design Suite Project Flow – Explains what Tcl commands are executed in a Vivado Design Suite project flow.
- Tcl Syntax and Structure – Understand the Tcl syntax and structure.

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