# Designing FPGAs Using the Vivado Design Suite 1

FPGA 1

FPGA-VDES1-ILT (v1.0)

**Course Specification**

## Course Description

This course offers introductory training on the Vivado® Design Suite and helps you to understand the FPGA design flow.

For those uninitiated to FPGA design, this course helps in designing an FPGA design, which includes creating a Vivado Design Suite project with source files, simulating the design, performing pin assignments, applying basic timing constraints, synthesizing, implementing, and debugging the design. Finally, the process for generating and downloading bitstream on a demo board is also covered.

**Level** – FPGA 1

**Course Duration** – 2 days

**Price** – $1400 or 14 Xilinx Training Credits

**Course Part Number** – FPGA-VDES1-ILT

**Who Should Attend?** – Digital designers new to FPGA design who need to learn the FPGA design cycle and the major aspects of the Vivado Design Suite

**Prerequisites**

- Basic knowledge of the VHDL or Verilog language
- Digital design knowledge

**Recommended Recorded Videos**

- Basic FPGA Architecture: Slice and I/O Resources*
- Basic FPGA Architecture: Memory and Clocking Resources*

**Software Tools**

- Vivado Design or System Edition 2016.3

**Hardware**

- Architecture: UltraScale™ and 7 series FPGAs**
- Demo board (optional): Kintex® UltraScale FPGA KCU105 board or Kintex-7 FPGA KC705 board**

* Go to www.xilinx.com/training and click the Online Training tab to view these videos.

** This course focuses on the UltraScale and 7 series architectures. The number of topic modules provided is greater than can be covered in two days. The instructor will select modules covered in class. Check with North Pole Engineering, Inc., for the specifics of in-class lab board and other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use the New Project Wizard to create a new Vivado IDE project
- Describe the supported design flows of the Vivado IDE
- Generate a DRC report to detect and fix design issues early in the flow
- Use the Vivado IDE I/O Planning layout to perform pin assignments
- Synthesize and implement the HDL design
- Apply clock and I/O timing constraints and perform timing analysis
- Describe the "baselining" process to gain timing closure on a design
- Use the Schematic and Hierarchy viewers to analyze and cross-probe a design
- Use the Vivado logic analyzer and debug flows to debug a design

## Course Outline

**Day 1**

- Introduction to FPGA Architecture, 3D IC, SoC {Lecture}
- UltraFast Design Methodology Introduction {Lecture, Demo}
- Introduction to Vivado Design Flows {Lecture}
- Vivado Design Suite Project-Based Mode {Lecture, Lab}
- Introduction to Digital Coding Guidelines {Lecture}
- Synthesis and Implementation {Lecture, Lab}
- Vivado Design Rule Checks {Lab}
- Timing Constraints Wizard {Lecture, Lab}
- Timing Constraints Editor {Lecture}
- Report Clock Networks {Lecture, Demo}
- Introduction to Clock Constraints {Lecture, Lab, Demo}
- Vivado Design Suite I/O Pin Planning {Lecture, Lab}
- I/O Constraints and Virtual Clocks {Lecture, Lab}

**Day 2**

- Basic Design Analysis in the Vivado IDE {Lab, Demo}
- Setup and Hold Timing Analysis {Lecture}
- Introduction to Vivado Timing Reports {Lecture, Demo}
- Vivado IP Flow {Lecture, Lab, Demo}
- Xilinx Power Estimator Spreadsheet {Lecture, Lab}
- Introduction to the Vivado Logic Analyzer {Lecture, Demo}
- HDL Instantiation Flow {Lecture, Lab}
- Introduction to Triggering {Lecture}
- Netlist Insertion Flow {Lecture, Lab}
- Debug Cores {Lecture}
- Introduction to the Tcl Environment {Lecture, Lab}
- Using Tcl Commands in the Vivado Design Suite Project Flow {Lecture, Demo}
- Tcl Syntax and Structure {Lecture}

## Topic Descriptions

**Day 1**

- Introduction to FPGA Architecture, 3D IC, SoC – Overview of FPGA architecture, SSI technology, and SoC device architecture.
- UltraFast Design Methodology Introduction – Introduces the methodology guidelines covered in this course and the UltraFast Design Methodology checklist.
- Introduction to Vivado Design Flows – Introduces the Vivado design flows: the project flow and non-project batch flow.
- Vivado Design Suite Project-Based Mode – Create a project, add files to the project, explore the Vivado IDE, and simulate the design.
- Introduction to Digital Coding Guidelines – Covers basic digital coding guidelines used in an FPGA design.
- Synthesis and Implementation – Create timing constraints according to the design scenario and synthesize and implement the design. Optionally, generate and download the bitstream to the demo board.
- Vivado Design Rule Checks – Run a DRC report on the elaborated design to detect design issues early in the flow. Fix the DRC violations.
- Timing Constraints Wizard – Use the Timing Constraints Wizard to apply missing timing constraints in a design.
- Timing Constraints Editor – Introduces the timing constraints editor tool to create timing constraints.
- Report Clock Networks – Use `report clock networks` to view the primary and generated clocks in a design.
- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.
- Vivado Design Suite I/O Pin Planning – Use the I/O Pin Planning layout to perform pin assignments in a design.
- I/O Constraints and Virtual Clocks – Apply I/O constraints and perform timing analysis.

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**Day 2**

- Basic Design Analysis in the Vivado IDE – Use the various design analysis features in the Vivado Design Suite.
- Setup and Hold Timing Analysis – Understand setup and hold timing analysis.
- Introduction to Vivado Timing Reports – Generate and use Vivado timing reports to analyze failed timing paths.
- Vivado IP Flow – Customize IP, instantiate IP, and verify the hierarchy of your design IP.
- Xilinx Power Estimator Spreadsheet – Estimate the amount of resources and default activity rates for a design and evaluate the estimated power calculated by XPE.
- Introduction to the Vivado Logic Analyzer – Overview of the Vivado logic analyzer for debugging a design.
- HDL Instantiation Flow – Covers the HDL instantiation flow to create and instantiate a VIO core and observe its behavior using the Vivado logic analyzer.
- Introduction to Triggering – Introduces the trigger capabilities of the Vivado logic analyzer.
- Netlist Insertion Flow – Use the Netlist Insertion flow to insert ILA cores into an existing synthesized netlist and debug a common problem.
- Debug Cores – Understand how the debug hub core is used to connect debug cores in a design.
- Introduction to the Tcl Environment – Introduces Tcl (tool command language).
- Using Tcl Commands in a Vivado Design Suite Project Flow – Explains what Tcl commands are executed in a Vivado Design Suite project flow.
- Tcl Syntax and Structure – Understand the Tcl syntax and structure.

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