Designing with the UltraScale and UltraScale+ Architectures

FPGA 3

FPGA-US-ILT (v1.0)

Course Specification

Course Description

This course introduces new and experienced designers to the most sophisticated aspects of the UltraScale™ and UltraScale+ architectures. Targeted towards designers who have used the Vivado® Design Suite, this course focuses on designing for the new and enhanced resources found in our new FPGA families.

Topics covered include an introduction to the UltraScale architecture CLB resources, the clock management resources (MMCM and PLL), global and regional clocking resources, memory and DSP resources, and source-synchronous resources. A description of the improvements to the dedicated transceivers and Transceiver Wizard is also included. Use of the Memory Interface Generator (MIG) and the new DDR4 memory interface capabilities is also covered.

In addition, you will learn how to best migrate your design and IP to the UltraScale architecture and the best way to use the Vivado Design Suite during design migration. A combination of modules and labs allow for practical hands-on experience of the principles taught.

Level – FPGA 3

Course Duration – 2 days

Price – $1400 or 14 Xilinx Training Credits

Course Part Number – FPGA-US-ILT

Who Should Attend? – Anyone who would like to build a design for the UltraScale or UltraScale+ device family

Prerequisites

- *Designing FPGAs Using the Vivado Design Suite 1* course
- Intermediate VHDL or Verilog knowledge

Software Tools

- Vivado HL Design or System Edition 2016.3

Hardware

- Architecture: UltraScale and UltraScale+ FPGAs*
- Demo board: KCU105 (if time permits)

* This course focuses on the UltraScale and UltraScale+ architectures. Check with your local Authorized Training Provider for specifics or other customizations. Check with North Pole Engineering, Inc., for specifics or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Take advantage of the primary UltraScale architecture resources
- Describe the new CLB capabilities and the impact that they make on your HDL coding style
- Define the block RAM, FIFO, and DSP resources available
- Describe the UltraRAM features
- Properly design for the I/O and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included
- Identify the hard IP resources available for implementing high-performance DDR4 memory interfaces
- Describe the additional features of the dedicated transceivers
- Effectively migrate your IP and design to the UltraScale architecture as quickly as possible

Course Outline

Day 1

- Introduction to the UltraScale Architecture {Lecture}
- UltraScale Architecture CLB Resources {Lecture, Lab}
- HDL Coding Techniques {Lecture, Lab}
- UltraScale Architecture Clocking Resources {Lectures, Lab}
- FPGA Design Migration {Lecture, Lab}
- Clocking Migration {Lab}
- UltraScale Architecture Block RAM Memory Resources {Lecture}
- UltraScale Architecture FIFO Memory Resources {Lecture}
- UltraRAM Memory {Lecture, Lab}
- UltraScale Architecture DSP Resources {Lecture}

Day 2

- Design Migration Software Recommendations {Lecture}
- DDR3 MIG Design Migration {Lab}
- DDR4 Design Creation Using MIG {Lab}
- UltraScale Architecture I/O Resources Overview {Lecture}
- UltraScale Architecture I/O Resources – Component Mode {Lecture, Lab}
- UltraScale Architecture I/O Resources – Native Mode {Lecture, Lab}
- Design Migration Methodology {Lecture}
- 10G PCS/PMA and MAC Design Migration {Lab}
- UltraScale Architecture Transceivers {Lecture, Lab}
- UltraScale FPGAs Transceivers Wizard {Lecture, Lab, Demo}
- Introduction to the UltraScale+ Families {Lecture}

Topic Descriptions

Day 1

- Introduction to the UltraScale Architecture – Review the UltraScale architecture, which includes enhanced CLB resources, DSP resources, etc.
- UltraScale Architecture CLB Resources – Examine the CLB resources, such as the LUT and the dedicated carry chain in the UltraScale architecture.
- HDL Coding Techniques – Analyze a design that has asynchronous resets by generating various reports, such as the Timing Summary report and Utilization report. Convert the asynchronous resets to synchronous resets by removing the reset signal from the sensitivity list.
- UltraScale Architecture Clocking Resources – Use the Clocking Wizard to configure a clocking subsystem to provide various clock outputs and distribute them on the dedicated global clock networks.
- FPGA Design Migration – Migrate an existing 7 series design to the UltraScale architecture.
- Clocking Migration – Migrate a 7 series design to the UltraScale architecture with a focus on clocking resources.
- UltraScale Architecture Block RAM Memory Resources – Review the block RAM resources in the UltraScale architecture.
- UltraScale Architecture FIFO Memory Resources – Review the FIFO resources in the UltraScale architecture.
- UltraRam Memory – Use UltraRAM for a design requiring a larger memory size than block RAM.
- UltraScale Architecture DSP Resources – Review the DSP Resources in the UltraScale architecture.

Day 2

- Design Migration Software Recommendations – List the Xilinx software recommendations for design migrations from 7 series to the UltraScale architecture.
- DDR3 MIG Design Migration – Migrate a 7 series MIG design to the UltraScale architecture.
- DDR4 MIG Design Creation – Create a DDR4 memory controller with the Memory Interface Generator (MIG) utility.
- UltraScale Architecture I/O Resources Overview – Review the I/O resources in the UltraScale architecture.
- UltraScale Architecture I/O Resources - Component Mode – Implement a high-performance, source-synchronous interface using I/O resources in Component mode for the UltraScale architecture.

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- UltraScale I/O Resources - Native Mode – Implement a high-performance, source-synchronous interface using I/O resources in Native mode for the UltraScale architecture.
- Design Migration Methodology – Review the migration methodology recommended by Xilinx for design migrations.
- 10G PCS/PMA and MAC Design Migration – Migrate a successfully implemented 7 series design containing the 10G Ethernet MAC and 10G PCS/PMA IP to an UltraScale FPGA.
- UltraScale Architecture Transceivers – Review the enhanced features of the transceivers in the UltraScale architecture.
- UltraScale FPGAs Transceivers Wizard – Use the Transceivers Wizard to build a design that uses a single serial transceiver and observe the created file structures.
- Introduction to the UltraScale+ Families – Identify the enhancements made to the UltraScale architecture in the UltraScale+ architecture families.

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