Course Description

This course will update experienced ISE® software users to utilize the Vivado® Design Suite. Learn the underlying database and static timing analysis (STA) mechanisms. Utilize Tcl for navigating the design, creating Xilinx design constraints (XDC), and creating timing reports. Learn to make appropriate timing constraints for SDR, DDR, source-synchronous, and system-synchronous interfaces for your FPGA design.

You will also learn to make path-specific, false path, and min/max timing constraints, as well as learn about timing constraint priority in the Vivado timing engine. Finally, you will learn about the scripting environment of the Vivado Design Suite and how to use the project-based scripting flow.

You will also learn the FPGA design best practices and skills to be successful using the Vivado Design Suite. This includes the necessary skills to improve design speed and reliability, including: system reset design, synchronization circuits, optimum HDL coding techniques, and timing closure techniques using the Vivado software. This course encapsulates this information with an UltraFast™ design methodology case study. The UltraFast design methodology checklist is also introduced.

Level – FPGA 4
Course Duration – 3 days
Price – $2700 or 27 Xilinx Training Credits
Course Part Number – FPGA-STAXDCADV-ILT
Who Should Attend? – Experienced FPGA designers (ISE or competitor)

Prerequisites

- Intermediate VHDL or Verilog knowledge
- FPGA design experience with Vivado or competing tools.
- New FPGA designers may wish to consider the following courses instead:
  - Designing FPGAs Using the Vivado Design Suite 1
  - Designing FPGAs Using the Vivado Design Suite 2
  - Designing FPGAs Using the Vivado Design Suite 3

Alternative training

- Designing FPGAs Using the Vivado Design Suite 4
- Vivado Design Suite Advanced XDC and STA for ISE Software Users

Software Tools
- Vivado Design or System Edition 2017.1

Hardware
- Architecture: UltraScale™ and 7 series FPGAs*
- Demo board: KCU105 and/or KC705

* This course focuses on the UltraScale and 7 series architectures. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Access primary objects from the design database and filter lists of objects using properties
- Describe setup and hold checks and describe the components of a timing report
- Create appropriate input and output delay constraints and describe timing reports that involve input and output paths
- Explain the impact that manufacturing process variations have on timing analysis and describe how min/max timing analysis information is conveyed in a timing report
- Describe all of the options available with the report_timing and report_timing_summary commands
- Describe the timing constraints required to constrain system-synchronous and source-synchronous interfaces

Course Outline

This course provides the student with much more material than can be covered in three days. Student consensus and/or time constraints may result in dynamic changes to the agenda.

Day 1
- Static Timing Analysis and Metastability (Lecture)
- Create Clock using four methods (Demo)
- Timing Constraint Wizard (Lecture/Demo)
- Timing Constraint Editor (Lecture/Demo)
- Clocking Wizard (Demo)
- Constraint sets (Demo)
- Long Lab 1: System and source synchronous timing with readable/maintainable constraints.

Day 2
- Optional: Vivado Logic Analyzer Insertion flow (Demo, Lab continuation)
- Report Datasheet (Lecture, Demo)
- Baselining (Lecture, Lab, Demo)
- Introduction to Timing Exceptions (Lecture, Lab, Demo)
- ASYNC_REG, HARD_SYNC, MTBF for 7-series and UltraScale (Demo)
- Report Clock Interaction (Lecture, Demo)
- Report Clock Networks (Lecture, Demo)

Day 3
- Scripting in Vivado Design Suite Non-Project Mode (Lecture, Lab)
- Hierarchical Design (Lecture)
- Managing Remote IP (Lecture, Lab)
- Timing Constraints Priority (Lecture)
- Introduction to Floorplanning (Lecture)
- Design Analysis and Floorplanning (Lecture, Lab)
- Incremental Compile Flow (Lecture, Lab)
- Physical Optimization (Lecture, Lab)
- Incremental Compile Flow (Lecture, Lab)

Self-study

The following material is also provided to the student. Material not covered above may be used for self-study (SS) or to refresh your memory on some of the more esoteric techniques covered below.

SS Day 1
FPGA-STATXDCADV-ILT (v1.0)

Course Specification

Topic Descriptions

Day 1

- UltraFast Design Methodology: Design Closure – Introduces the UltraFast™ methodology guidelines on design closure.
- UltraFast Design Methodology: Advanced Techniques – Introduces the methodology guidelines for advanced techniques.
- Timing Constraints Wizard – Use the Timing Constraints Wizard to apply missing timing constraints in a design.
- Timing Constraints Editor – Introduces the timing constraints editor tool to create timing constraints.
- Introduction to Vivado Reports – Generate and use Vivado timing reports to analyze timing paths.
- Introduction to Clock Constraints – Apply clock constraints and perform timing analysis.

Day 2

- Synchronization Circuits – Use synchronization circuits for clock domain crossings.
- Report Datasheet – Use the datasheet report to find the optimal setup and hold margin for an I/O interface.
- Baselining – Use Xilinx-recommended baselining procedures to progressively meet timing closure.
- Pipelining – Use pipelining to improve design performance.
- I/O Timing Scenarios – Overview of various I/O timing scenarios, such as source- and system-synchronous, direct/MMCM capture, and edge/center aligned data.
- Source-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a source-synchronous, double data rate (DDR) interface.
- System-Synchronous I/O Timing – Apply I/O delay constraints and perform static timing analysis for a system-synchronous input interface.
- Timing Constraints Priority – Identify the priority of timing constraints.
- Case Analysis – Understand how to analyze timing when using multiplexed clocks in a design.
- Introduction to Floorplanning – Introduction to floorplanning and how to use Pblocks while floorplanning.
- Physical Optimization – Use physical optimization techniques for timing closure.

Day 3

- UltraFast Design Methodology: Advanced Techniques – Introduces the UltraFast™ design methodology guidelines covered in this course.
- Scripting in Vivado Design Suite Non-Project Mode – Write Tcl commands in the non-project batch flow for a design.

Day 4

- Physical Optimization (Lecture, Lab)
- Vivado Design Suite ECO Flow (Lecture, Lab)
- Power Management Techniques (Lecture)
- Daisy Chains and Gans in Configuration (Lecture)
- Bitstream Security (Lecture, Lab)
- Vivado Design Suite Debug Methodology (Lecture)
- Trigger and Debug at Device Startup (Lecture, Demo)
- Debugging the Design Using Tcl Commands (Lecture, Lab)
- Using Procedures in Tcl Scripting (Lecture)
- Using Lists in Tcl Scripting (Lecture)
- Using regexp in Tcl Scripting (Lecture, Lab)
- Debugging and Error Management in Tcl Scripting (Lecture)
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Course Specification

Visit www.npe-inc.com/training, for full course schedule and training information.

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
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- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

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