Xilinx Partial Reconfiguration Tools and Techniques

FPGA 4

FPGA-PR-ILT (v1.0)

Course Specification

Course Description

This course demonstrates how to use the Vivado® Design Suite to construct, implement, and download a Partially Reconfigurable (PR) FPGA design. You will gain a firm understanding of PR technology and learn how successful PR designs are completed. You will also identify best design practices and understand the subtleties of the PR design flow. This course also demonstrates how to use thee PR controller and PR decoupler IP in the PR process. You will also gain an understanding of PR implementation in an embedded system environment.

This course covers both the tool flow and mechanics of successfully creating a PR design. This course also covers both UltraScale™ and 7 series architecture design requirements, recommendations, and expectations for PR systems. In addition, it describes several techniques focusing on appropriate coding styles for a PR system as well as system-level design considerations and practical applications. You will also identify techniques to debug PR designs.

Level – FPGA 4

Course Duration – 2 days

Price – $1800 or 18 Xilinx Training Credits

Course Part Number – FPGA-PR-ILT

Who Should Attend? – Digital designers who have a working knowledge of HDL (VHDL or Verilog) and the Xilinx design methodology and who have need of partial reconfiguration techniques

Prerequisites

- Designing FPGAs with the Vivado Design Suite 2 course
- Designing FPGAs with the Vivado Design Suite 3 course
- Designing FPGAs with the Vivado Design Suite 4 course
- Working HDL knowledge (VHDL or Verilog)

Software Tools

- Vivado Design or System Edition 2017.1

Hardware

- Architecture: UltraScale and 7 series FPGAs*
- Demo board: Kintex® UltraScale FPGA KCU105 board, Kintex-7 FPGA KC705 board, and ZedBoard**

* This course focuses on the UltraScale and 7 series architectures. Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations.

** The UltraScale architecture versions of the "Using the PRC IP in a Partial Reconfiguration Design" lab and the "Using ILA Cores to Debug Partial Reconfiguration Designs" lab are not available because of QSPI and PRC issues on the KCU105 board. These two labs support only the 7 series architecture. The "Partial Reconfiguration in Embedded Systems" lab requires a ZedBoard for implementation.

After completing this comprehensive training, you will have the necessary skills to:

- Build and assemble a Partially Reconfigurable system (UltraScale, 7 series, and Zynq® devices)
- Define PR regions and reconfigurable modules with the Vivado Design Suite
- Generate the appropriate full and partial bitstreams for a PR design
- Use the ICAP and PCAP components to deliver the partially reconfigurable systems
- Identify how Partial Reconfiguration affects various silicon resources, including block RAM, IOBs, fabric, clock buffers, and MGTs
- Implement a Partial Reconfiguration system using the following techniques:
  - Direct JTAG connection
  - Floorplanning
  - Timing constraints and analysis
- Implement a PR system using the PRC IP
- Implement a PR system in an embedded environment
- Debug PR designs

Course Outline

Day 1

- Introduction to Partial Reconfiguration
- **Demo:** Introduction to Partial Reconfiguration
- Partial Reconfiguration Flow
- **Lab 1:** Partial Reconfiguration Tool Flow
- **Lab 2:** Partial Reconfiguration Project Flow
- **Lab 3:** Floorplanning the PR Design
- Partial Reconfiguration Design Considerations
- Optional: FPGA Configuration Overview
- Partial Reconfiguration Bitstreams
- **Demo:** Partial Reconfiguration Controller (PRC) IP
- **Lab 4:** Using the Partial Reconfiguration Controller in a PR Design

Day 2

- Partial Reconfiguration: Managing Timing
- **Lab 5:** Partial Reconfiguration Timing Analysis and Constraints
- Partial Reconfiguration in Embedded Systems
- **Lab 6:** Partial Reconfiguration in Embedded Systems
- Debugging Partial Reconfiguration Designs
- **Lab 7:** Debugging a Partial Reconfiguration Design
- Partial Reconfiguration Design Recommendations
- PCIe Core and Partial Reconfiguration

Lab Descriptions

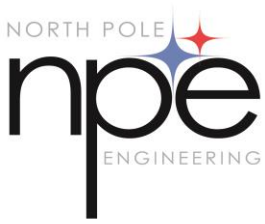
- **Lab 1:** Partial Reconfiguration Tool Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- **Lab 2:** Partial Reconfiguration Project Flow – Illustrates Partial Reconfiguration (PR) project flow in the Vivado® Design Suite. At the end of this lab, you will be able to create multiple RMs and configurations using Partial Reconfiguration Wizard.
- **Lab 3:** Floorplanning the PR Design – Illustrates how to create efficient Pblocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.
- **Lab 4**: Using the Partial Reconfiguration Controller in a PR Design – Illustrates using the PRC IP and hardware triggers to manage partial bitstreams.
- **Lab 5:** Partial Reconfiguration Timing Analysis and Constraints – Shows how area groups and Reconfigurable Partitions affect design performance.
- **Lab 6**: Partial Reconfiguration in Embedded Systems – Illustrates implementing PR designs in an embedded environment.
- **Lab 7**: Debugging a Partial Reconfiguration Design – Demonstrates using ILA cores to debug PR designs and shows which signals to monitor during debugging.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

© 2017 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and disclaimers are as listed at http://www.xilinx.com/legal.htm.
All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.

Visit **www.npe-inc.com/training**, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent here.

NPE Course Cancellation Policy

- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

© 2017 Xilinx, Inc. All rights reserved. All Xilinx trademarks, registered trademarks, patents, and disclaimers are as listed at http://www.xilinx.com/legal.htm.
All other trademarks and registered trademarks are the property of their respective owners. All specifications are subject to change without notice.