

Course Description

Attending the *FPGA Power Optimization* class will help you create a more power efficient FPGA design. This course can help you fit your design into a smaller FPGA, reduce your FPGA's power consumption, or run your FPGA at a lower temperature. In addition, by mastering the tools and design methodologies presented in this course, you will be able to create your design faster, shorten your development time, and lower development costs.

Level – FPGA 2

Course Duration – 1 day

Price – \$600 or 6 Xilinx Training Credits

Course Part Number – FPGA24000-13-ILT

Who Should Attend? – FPGA designers with intermediate knowledge of HDL and some experience with the Xilinx ISE® software tools

Prerequisites

- *Essentials of FPGA Design* course or equivalent knowledge of FPGA architecture features; the Xilinx implementation software flow and implementation options; reading timing reports; basic FPGA design techniques; global timing constraints and the Constraints Editor
- Intermediate HDL knowledge (VHDL or Verilog)
- Solid digital design background

Recommended

- *Designing for Performance* course
- Basic FPGA Architecture: Memory and Clocking Resources

Software Tools

- Xilinx ISE Design Suite: Logic or System Edition 13.1

Hardware

- Architecture: 7 series FPGAs*
- Demo board: Virtex®-6 FPGA ML605 board*

** This course focuses on the 7 series FPGA architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Use Xilinx Power Estimator spreadsheet to estimate your design's power consumption at the concept phase
- Use the Xilinx Power Analyzer to estimate your design's power consumption after implementation has been completed
- Import Activity Rates to complete a dynamic power estimation
- Use the synthesis and implementation options to reduce your design's power consumption
- Use optimum HDL coding techniques and design practices to reduce your design's power consumption
- Take advantage of the Virtex-7 architecture features that reduce power consumption

Course Outline

- Introduction
- FPGA Power Requirements
- Xilinx Power Estimator Spreadsheet (XPE)
- **Lab 1:** Power Estimation with XPE
- Xilinx Power Analyzer
- **Lab 2:** Power Estimation with XPA
- **Lab 3:** Dynamic Power Estimation
- Power Management Software Options

- **Lab 4:** Power Management Software Options
- Power Management Design Techniques
- Power Optimization of I/O Resources
- 7 Series Power Management Features
- How to Solve a Power Problem
- Worse-Case Thermal Calculations (optional)
- Spartan-6 FPGA Power Management Features (optional)
- Virtex-6 FPGA Power Management Features (optional)
- Power and Temperature Measurement Features (optional)
- Introduction to Partial Reconfiguration (optional)

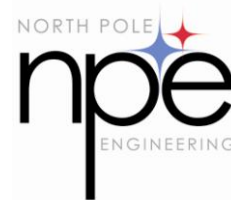
Lab Descriptions

- **Lab 1:** Power Estimation with XPE – Estimate the resources required based on the high-level design description. Enter the amount of resources and default activity rates for the design and evaluate the estimated power calculated by XPE.
- **Lab 2:** Power Estimation with XPA – Import the MAP report contents into the XPE spreadsheet and evaluate the estimated power with the XPE. Estimate the design's power consumption with the XPA power estimation utility and compare its results to that made with XPE.
- **Lab 3:** Dynamic Power Estimation – Simulate the design with ISim and generate the necessary Switching Activity Interchange Format (SAIF) file. Launch the XPA utility, load the SAIF file contents, and use XPA to estimate your design's dynamic power consumption.
- **Lab 4:** Power Management Software Options – Use the Power reduction option in MAP and the Global Optimization settings to save power in your design.

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