Zynq® Boot Camp

Embedded Master 4

EMBD44040-ILT (v1.0)

Course Specification

Course Description

The Xilinx Zynq® All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This advanced custom course based on Xilinx and North Pole Engineering labs provides system architects with the knowledge to architect and implement a Zynq All Programmable SoC.

Zynq SoC Master training presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

Zynq SoC Master training details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL. The course also includes self-study labs for using the MicroBlaze in other 7-series and UltraScale FPGAs.

Build an effective FPGA design using synchronous design techniques, instantiate appropriate device resources, use proper HDL coding techniques, make good pin assignments, set basic XDC timing constraints, and use the Vivado® Design Suite to build, synthesize, implement, and download a design.

Level – Embedded Architect 4

Course Duration – 5 days

Price – $4100 or 41 Xilinx Training Credits

Optional ZedBoard Purchase – $495

Optional ZC702 Purchase – $895

Course Part Number – EMBD44040-ILT

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC.

Prerequisites

- FPGA design experience (VHDL/Verilog)
- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2014.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC Zed board and/or Kintex®-7 FPGA KC705 board*

* This course focuses on the Zynq-7000 All Programmable SoC. Check with North Pole Engineering, Inc., for specifics of the in-class lab board or other customizations.

After completing this training, you will have the necessary resources to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL
- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a MicroBlaze™ or Cortex™-A9 processor using the Vivado IP Integrator and Customization Wizard
- Develop software applications utilizing the Eclipse-based Software Development Kit (SDK)
- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Take advantage of the primary 7 series FPGA architecture resources
- Troubleshoot software and hardware using the SDK and Vivado Logic analyzer simultaneously.
- Identify the available Vivado IDE design flows (project based and non-project batch)
- Identify file sets (HDL, XDC, simulation)
- Analyze designs by using the cross-selection capabilities, Schematic viewer, and Hierarchical viewer
- Synthesize and implement an HDL design
- Utilize the available synthesis and implementation reports to analyze a design (utilization, timing, power, etc.)
- Build custom IP with the IP Library utility
- Make basic timing constraints (create_clock, set_input_delay, and set_output_delay)
- Use the primary Tcl-based reports (check_timing, report_clock_interaction, report_clock_networks, and report_timing_summary)
- Describe and analyze common STA reports
- Identify synchronous design techniques
- Describe how a 7 series FPGA is configured

Course Outline

You will be provided printed materials and labs for the full 6 days' worth of course, but the instructor will present only 5 days' worth of materials and labs from the following, and other custom labs/demos.

Day 1

- UltraFast Design Methodology Summary
- Basic FPGA Architecture
- Introduction to the Vivado Design Suite
- Vivado Design Flows
- Demo: Visualization for Analysis
- **Lab 1**: Vivado Tool Overview
- Designing with IP
- Basic Timing Constraints and Reports
- **Lab 2:** Vivado Synthesis, Implementation, and Timing Closure

Day 2

- Designing with FPGA Resources
- Clocking Resources
- **Lab 3a:** Designing with FPGA Resources
- **Lab 3b:** Designing with IP – IP Integrator Flow
- Basic Timing Constraints (XDC)
- Timing Reports
- **Lab 4:** Basic XDC and Timing Reports
- Synchronous Design Techniques

- 7-Series FPGA Configuration

Day 3

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1: Extended student/Instructor demonstration and follow along lab:** Investigate AXI bus, AXI interconnect, DMA performance, and tips and tricks of Vivado Logic Analyzer. Benchmark DMA performance. Understand relationship between settings in IP Integrator and SDK drivers/headers/APIs.

Day 4

- Formal Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- Programmable SoC
- Zynq All Programmable SoC Booting
- Zynq All Programmable SoC Memory Resources
- **Lab 2:** Debugging on the Zynq All Programmable SoC

Day 5

- Meeting Performance Goals
- Embedded Design Overview
- IP Integrator and the PS Configuration Wizard
- **Lab 3: Extended student/Instructor Demonstration and follow along lab**. Integrating a simple, highly illustrative piece of IP into AXI, with cross functional troubleshooting. Troubleshoot using SDK, Vivado XSIM, Vivado Logic Analyzer, and/or digital oscilloscope. Custom VHDL and lab instructions included.
- **Optional Instructor Demonstration**: Complex multi-AXI interface IP design. Read DMA, AXI-Lite, and AXI-FULL in a hardware SVGA driver. This demonstration usually takes runs after completion of the normal course, and is optional for engineering students.

In addition to the above, you will receive the following printed materials and labs that can be completed self-study (SS) after class:

- Custom Xilinx and ARM Acronyms and Initialisms list (MS Word or PDF format)

SS Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- **SSLab 1:** Building a Zynq All Programmable SoC Platform
- Processor Input/Output Peripherals
- Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- **SSLab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- Zynq All Programmable SoC Booting

SS Day 2

- Zynq All Programmable SoC Memory Resources
- Meeting Performance Goals
- **SSLab 3:** Using DMA on the Zynq All Programmable SoC
- Zynq All Programmable SoC Hardware Design
- Zynq All Programmable SoC Software Design
- Debugging the Zynq All Programmable SoC
- **SSLab 4:** Debugging on the Zynq All Programmable SoC
- Zynq All Programmable SoC Tools and Reference Designs
- **SSLab 5:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

SS Day 3

- Embedded Design Overview
- IP Integrator and the PS Configuration Wizard
- **SSLab 6**: Hardware Construction Using the Vivado IP Integrator
- Software Development Using SDK
- **SSLab 7**: Adding and Downloading Software
- Introduction to AXI
- Interrupts
- Adding Hardware to an Embedded System
- **SSLab 8**: Adding IP to a Hardware Design

SS Day 4

- MicroBlaze Processor Basics
- Cortex-A9 Processor Basics
- Designing a Custom AXI Peripheral
- Using the Create and Package IP Wizard to Build a Custom AXI Peripheral
- **SSLab 9**: Building Custom AXI IP for an Embedded System
- Bus Functional Model Simulation
- **SSLab 10**: BFM Simulation - AXI Peripheral
- Adding Custom IP to the Embedded System
- **SSLab 11**: Integrating a Custom Peripheral

Self Study Lab Descriptions

You will be provided printed materials and labs for the full 4 day course, but the instructor will present only 3 days' worth of materials and labs including custom labs/demos.

- **SSLab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **SSLab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **SSLab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **SSLab 4:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **SSLab 5:** Running and Debugging a Linux Application on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.
- **SSLab 6:** Hardware Construction Using the Vivado IP Integrator – Create a project using the IP integrator to develop a basic hardware system and generate a series of netlists for the embedded design.
- **SSLab 7:** Adding and Downloading Software – Complete the processes begun in Lab 1 using the SDK tools to create a software BSP and sample application. Configure the device and download the application.
- **SSLab 8:** Adding IP to a Hardware Design – Add IP to an existing processing system. Configure the device and download the application.

- **SSLab 9:** Building Custom AXI IP for an Embedded System – Add a custom AXI peripheral to the Vivado IP catalog using the Create and Package IP Wizard.
- **SSLab 10:** BFM Simulation – AXI Peripheral – Test custom IP via bus functional model (BFM) simulation.
- **SSLab 11:** Integrating a Custom Peripheral – Add the custom IP created in Lab 4 to an existing processor system.

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