

Course Description

The Xilinx Zynq® All Programmable System on a Chip (SoC) provides a new level of system design capabilities. This course provides system architects with the knowledge to effectively architect a Zynq All Programmable SoC.

Zynq SoC Master training presents the features and benefits of the Zynq architecture for making decisions on how to best architect a Zynq All Programmable SoC project. It covers the architecture of the ARM® Cortex™-A9 processor-based processing system (PS) and the connections to the programmable logic (PL) at a sufficiently deep level that a system designer can successfully and effectively utilize the Zynq All Programmable SoC.

Zynq SoC Master training details the individual components that comprise the PS: I/O peripherals, timers, caching, DMA, interrupt, and memory controllers. Emphasis is placed on effective access and usage of the PS DDR controller from PL user logic, efficient PL-to-PS interfacing, and design techniques, tradeoffs, and advantages of implementing functions in the PS or the PL. The course also includes self-study labs for using the MicroBlaze in other 7-series and UltraScale FPGAs.

Level – Embedded Architect 3

Course Duration – 3 days

Price – \$2700 or 27 Xilinx Training Credits

Course Part Number – EMBD-ZSA-ILT

Who Should Attend? – System architects who are interested in architecting a system on a chip using the Zynq All Programmable SoC.

Prerequisites

- Digital system architecture design experience
- Basic understanding of microprocessor architecture
- Basic understanding of C programming
- Basic HDL modeling experience

Software Tools

- Vivado® Design or System Edition 2015.1

Hardware

- Architecture: Zynq-7000 All Programmable SoC*
- Demo board: Zynq-7000 All Programmable SoC ZedBoard and/or Kintex®-7 FPGA KC705 board**

* This course focuses on the Zynq-7000 All Programmable SoC. Check with North Pole Engineering, Inc., for specifics of the in-class lab board or other customizations. ZedBoard provided in class use for in person training. ZedBoards or ZC702 cards are also available for purchase from North Pole Engineering as part of this training for additional fee on the same invoice. Contact North Pole Engineering for more information.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the architecture and components that comprise the Zynq All Programmable SoC processing system (PS)
- Relate a user design goal to the function, benefit, and use of the Zynq All Programmable SoC
- Effectively select and design an interface between the Zynq PS and programmable logic (PL) that meets project goals
- Analyze the tradeoffs and advantages of performing a function in software versus PL
- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a MicroBlaze™ or Cortex™-A9 processor using the Vivado IP Integrator and Customization Wizard
- Develop software applications utilizing the Eclipse-based Software Development Kit (SDK)
- Create and integrate an IP-based processing system component in the Vivado Design Suite

- Design and add a custom AXI interface-based peripheral to the embedded processing system

Course Outline

You will be provided printed materials and labs for the full 4 day course, but the instructor will present only 3 days' worth of materials and labs from the following, and other custom labs/demos only available through North Pole Engineering, Inc. training.

Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- Processor Input/Output Peripherals
- **Lab 1: Extended student/Instructor demonstration and follow along lab:** Investigate AXI bus, AXI interconnect, DMA performance, and tips and tricks of Vivado Logic Analyzer. Benchmark DMA performance. Understand relationship between settings in IP Integrator and SDK drivers/headers/APIs.

Day 2

- Formal Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- Programmable SoC
- Zynq All Programmable SoC Booting
- Zynq All Programmable SoC Memory Resources
- **Lab 2:** Debugging on the Zynq All Programmable SoC

Day 3

- Meeting Performance Goals
- Embedded Design Overview
- IP Integrator and the PS Configuration Wizard
- **Lab 3: Extended student/Instructor Demonstration and follow along lab.** Integrating a simple, highly illustrative piece of IP into AXI, with cross functional troubleshooting. Troubleshoot using SDK, Vivado XSIM, Vivado Logic Analyzer, and/or digital oscilloscope. Custom VHDL and lab instructions included.
- **Optional Instructor Demonstration:** Complex multi-AXI interface IP design. Read DMA, AXI-Lite, and AXI-FULL in a hardware SVGA driver. This demonstration usually takes runs after completion of the normal course, and is optional for engineering students.

In addition to the above, you will receive the following printed materials and labs that can be done after class:

SS Day 1

- Zynq All Programmable SoC Overview
- Inside the Application Processor Unit (APU)
- **Lab 1:** Building a Zynq All Programmable SoC Platform
- Processor Input/Output Peripherals
- Introduction to AXI
- Zynq All Programmable SoC PS-PL Interface
- **Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC
- Zynq All Programmable SoC Booting
- **Lab 3:** Using DMA on the Zynq All Programmable SoC

SS Day 2

- Zynq All Programmable SoC Memory Resources
- Meeting Performance Goals
- **Lab 4:** Impact of Port Selection on System Performance
- Zynq All Programmable SoC Hardware Design

EMBD33040-ILT (v1.0)

Course Specification

- Zynq All Programmable SoC Software Design
- Debugging the Zynq All Programmable SoC
- **Lab 5:** Debugging on the Zynq All Programmable SoC
- Zynq All Programmable SoC Tools and Reference Designs
- **Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC

SS Day 3

- Embedded Design Overview
- IP Integrator and the PS Configuration Wizard
- **Lab 7:** Hardware Construction Using the Vivado IP Integrator
- Software Development Using SDK
- **Lab 8:** Adding and Downloading Software
- Introduction to AXI
- Interrupts
- Adding Hardware to an Embedded System
- **Lab 9:** Adding IP to a Hardware Design

SS Day 4

- Designing a Custom AXI Peripheral
- Using the Create and Package IP Wizard to Build a Custom AXI Peripheral
- **Lab 10:** Building Custom AXI IP for an Embedded System
- Bus Functional Model Simulation
- **Lab 11:** BFM Simulation – AXI Peripheral
- MicroBlaze Processor Basics
- Zynq All Programmable SoC Processor Basics
- **Lab 12:** Testing Custom AXI IP on Hardware
- Managing Embedded System Design Projects
- **Lab 13:** Integrating a Custom Peripheral

Lab Descriptions

- **SS Lab 1:** Building a Zynq All Programmable SoC Platform – Examine the process of using the Vivado IP Integrator tool to create a simple processing system.
- **SS Lab 2:** Integrating Programmable Logic on the Zynq All Programmable SoC – Connect a programmable logic (PL) design to the embedded processing system (PS).
- **SS Lab 3:** Using DMA on the Zynq All Programmable SoC – Experiment with effectively using the PS DMA controller to move data between DDRx memory and a custom PL peripheral.
- **SS Lab 4:** Impact of Port Selection on System Performance – Explore bandwidth issues surrounding the use of the Accelerator Coherency Port (ACP) and the High Performance (HP) ports.
- **SS Lab 5:** Debugging on the Zynq All Programmable SoC – Evaluate debugging the hardware and software components of a Zynq All Programmable SoC design.
- **SS Lab 6:** Running and Debugging a Linux Application on the Zynq All Programmable SoC – Explore a software application executing under the Linux operating system on the Zynq All Programmable SoC.
- **SS Lab 7:** Hardware Construction Using the Vivado IP Integrator – Create a project using the IP integrator to develop a basic hardware system and generate a series of netlists for the embedded design.
- **SS Lab 8:** Adding and Downloading Software – Continuing from a completed hardware system, begin software development using the SDK tools to create a software BSP and sample application. Download and run the application.

- **SS Lab 9:** Adding IP to a Hardware Design – Add IP to an existing processing system. Configure the device and download the application.
- **SS Lab 10:** Building Custom AXI IP for an Embedded System – Add a custom AXI peripheral to the Vivado IP catalog using the Create and Package IP Wizard.
- **SS Lab 11:** BFM Simulation – AXI Peripheral – Test custom IP via bus functional model (BFM) simulation.
- **SS Lab 12:** Testing Custom AXI IP on Hardware – Use debug cores and the Vivado hardware manager to test custom IP.
- **SS Lab 13:** Integrating a Custom Peripheral – Add the custom IP created in Lab 4 to an existing processor system.

Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

Visit www.npe-inc.com/training, for full course schedule and training information.



You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.