

## Course Description

*Designing for Performance for CPLDs* is an intermediate-level course that provides a comprehensive overview of the CPLD software flow. By applying the techniques presented in this course, you will be able to enhance design performance and make the best possible use of Xilinx CPLD architectures.

This course uses the ISE™ 9.1 software, including the Constraints Editor and Timing Analyzer. Other topics include understanding the CPLD logic engine, estimating power, and fitting difficult designs.

**Level** – Intermediate

**Course Duration** – 1 day

**Price** –

**Course Part Number** – CPLD23000-9-ILT

**Who Should Attend?** – Digital designers who have working knowledge of basic HDL (VHDL or Verilog) and who have some experience designing with Xilinx CPLDs. Alternatively, those who have recently attended *Fundamentals of CPLD Design*.

### Prerequisites

- Basic HDL knowledge (VHDL or Verilog)
- Digital design knowledge and Xilinx CPLD experience
- *Fundamentals of CPLD Design* course or equivalent knowledge of CPLD architecture; Xilinx implementation software flow and options; global constraints, the Constraints Editor; and reading fitting and timing reports
- Some experience with the software tool flow and global timing constraints

### Software Tools

- Xilinx ISE 9.1i

After completing this comprehensive training, you will have the necessary skills to:

- Apply techniques to fit more logic into a device
- Describe the CoolRunner™-II CPLD timing model and how it can be used to analyze design performance
- Describe the advanced capabilities of the CoolRunner-II CPLD architecture
- Estimate the power consumption of a CPLD design

## Course Outline

- Course Agenda
- Review of Fundamentals of CPLD Design
- XST for CPLDs
- Advanced Fitting
- Handling No-Fit Situations
- **Lab 1:** Fitting
- CPLD Timing
- **Lab 2:** CPLD Timing
- CPLD Logic Engine
- Coding Techniques
- CPLD Best Design Practices
- Power Estimation

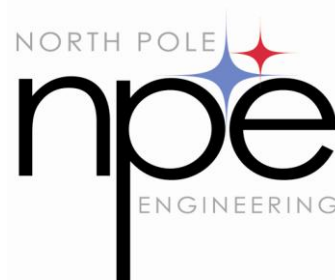
## Lab Descriptions

- **Lab 1:** Fitting – Apply the knowledge and techniques learned in the previous modules to fit designs into smaller devices.
- **Lab 2:** CPLD Timing – Analyze the timing of a design and create testbenches that can be simulated to verify the behavior of the design.

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