

### Course Description

The course provides a thorough introduction to the Vivado® High-Level Synthesis (HLS) tool. This course covers synthesis strategies, features, improving throughput, area, interface creation, latency, testbench coding, and coding tips. Utilize the Vivado HLS tool to optimize code for high-speed performance in an embedded environment and download for in-circuit validation.

**Level** – DSP 3

**Course Duration** – 2 days

**Price** – \$1400 or 14 Xilinx Training Credits

**Course Part Number** – DSP-HLS-ILT

**Who Should Attend?** – Software and hardware engineers looking to utilize high-level synthesis

#### Prerequisites

- C, C++, or System C knowledge
- High-level synthesis for software engineers OR high-level synthesis for hardware engineers

#### Software Tools

- Vivado System Edition 2015.3

#### Hardware

- Architecture: Zynq®-7000 All Programmable SoC and 7 series FPGAs\*
- Demo board: Zynq-7000 All Programmable SoC ZC702 or ZedBoard\*

\* This course focuses on the Zynq-7000 All Programmable SoC and 7 series FPGA architectures. Check with North Pole Engineering, Inc., for the specifics of the in-class lab board, other customizations, or private on site training.

After completing this comprehensive training, you will have the necessary skills to:

- Enhance productivity using the Vivado HLS tool
- Describe the high-level synthesis flow
- Use the Vivado HLS tool for a first project
- Identify the importance of the testbench
- Use directives to improve performance and area and select RTL interfaces
- Identify common coding pitfalls as well as methods for improving code for RTL/hardware
- Perform system-level integration of IP generated by the Vivado HLS tool
- Describe how to use OpenCV functions in the Vivado HLS tool

### Course Outline

#### Day 1

- Introduction to High-Level Synthesis and the Vivado HLS Tool
- Using the Vivado HLS Tool: GUI Flow
- Demo: Vivado HLS Tool Overview
- **Lab 1:** Introduction to the Vivado HLS Tool Flow
- Vivado HLS Tool Command Line Interface
- **Lab 2:** Introduction to the Vivado Tool HLS CLI Flow
- Optimizing for Latency
- **Lab 3:** The Impact of Unrolling Loops
- Optimizing for Throughput
- **Lab 4:** Optimizing for Throughput

#### Day 2

- Optimizing Arrays
- **Lab 5:** Handling Memories
- Optimizing for Area
- I/O Interfaces
- Demo: AXI4-Streaming Interfaces
- **Lab 6:** System Integration
- HLS UltraFast Design Methodology
- Vivado HLS Tool: C Code
- **Lab 7:** Matrix Multiplication

### Lab Descriptions

- **Lab 1:** Introduction to the Vivado HLS Tool Flow – Utilize the GUI to simulate and create a project. Perform RTL synthesis, verification, and exporting the C design as an IP.
- **Lab 2:** Introduction to the Vivado HLS Tool CLI Flow – Utilize a make file to perform C simulation. Create a project and perform C synthesis, RTL verification, and RTL packaging.
- **Lab 3:** The Impact of Unrolling Loops – Analyze multiple results of the design and apply directives to optimize loop latency.
- **Lab 4:** Optimizing for Throughput – Optimize loop performance and modify pipelining and its effect on performance.
- **Lab 5:** Handling Memories – Analyze the impact of manipulating arrays. Utilize directives to optimize the design for area.
- **Lab 6:** System Integration – Set up an embedded design, create an HLS IP with the AXI Lite interface, import the IP into the embedded design, and validate the system on the demo board.
- **Lab 7:** Matrix Multiplication – Write a C-code 3x3 matrix multiplier, verify the design, and apply directives to improve performance.

### Register Today

NPE, Inc. delivers public and private courses in locations throughout the central US region; including Iowa, Illinois, Kansas, Minnesota, Missouri, North Dakota, South Dakota and Wisconsin.

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You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

### Student Cancellation Policy

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- Student cancellations received less than 7 days before the first day of class are entitled to a 100% credit toward a future class.
- Student cancellations must be sent [here](#).

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- We regret from time to time classes will need to be rescheduled or cancelled.
- In the event of cancellation, live on-line training may be offered as a substitute.
- NPE may cancel a class up to 7 days before the scheduled start date of the class; all students will be entitled to a 100% refund.
- Under no circumstances is NPE responsible or liable for travel, lodging or other incidental costs. Please be aware of this cancellation policy when making your arrangements.
- For additional information or to schedule a private class contact us here.

This class is also available as a Guaranteed to Run (GTR) option. Please see [DSP21010 course specification](#) for more information.