DSP Design Using System Generator

DSP 3

DSP-SYSGEN-ILT (v1.0)

Course Specification

Course Description

This course allows you to explore the System Generator tool and to gain the expertise you need to develop advanced, low-cost DSP designs. This intermediate course in implementing DSP functions focuses on learning how to use System Generator for DSP, design implementation tools, and hardware co-simulation verification. Through hands-on exercises, you will implement a design from algorithm concept to hardware verification using the Xilinx FPGA capabilities.

Level – DSP 3

Course Duration – 2 days

Price – $1600 or 16 Xilinx Training Credits

Course Part Number – DSP-SYSGEN-ILT

Who Should Attend? – System engineers, system designers, logic designers, and experienced hardware engineers who are implementing DSP algorithms using the MathWorks MATLAB® and Simulink® software and want to use Xilinx System Generator for DSP design

Prerequisites

- Experience with the MATLAB and Simulink software
- Basic understanding of sampling theory

Recommend

- Essential DSP Implementation Techniques

Software Tools

- Vivado® System Edition 2016.3
- MATLAB with Simulink software R2016b

Hardware

- Architecture: 7 series and UltraScale™ FPGAs
- Demo board: Kintex®-7 FPGA KC705 board or Kintex UltraScale™ FPGA KCU105 board and Zynq®-7000 All Programmable SoC ZC702 or ZedBoard*

* Check with North Pole Engineering, Inc. for the specifics of the in-class lab board or other customizations. The ZC702 or ZedBoard (provided during course for in-person training) is utilized in the "AXI4-Lite Interface Synthesis" lab.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the System Generator design flow for implementing DSP functions
- Identify Xilinx FPGA capabilities and how to implement a design from algorithm concept to hardware simulation
- List various low-level and high-level functional blocks available in System Generator
- Run hardware co-simulation
- Identify the high-level blocks available for FIR and FFT designs
- Implement multi-rate systems in System Generator
- Integrate System Generator models into the Vivado IDE
- Design a processor-controllable interface using System Generator for DSP
- Generate IPs from C-based design sources for use in the System Generator environment

Course Outline

Day 1

- Introduction to System Generator
- Simulink Software Basics
- **Lab 1:** Using the Simulink Software
- Basic Xilinx Design Capture
- Demo: System Generator Gateway Blocks
- **Lab 2:** Getting Started with Xilinx System Generator
- Signal Routing
- **Lab 3:** Signal Routing
- Implementing System Control
- **Lab 4:** Implementing System Control

Day 2

- Multi-Rate Systems
- **Lab 5:** Designing a MAC-Based FIR
- Filter Design
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block
- System Generator, Vivado Design Suite, and Vivado HLS Integration
- **Lab 7:** System Generator and Vivado IDE Integration
- Kintex-7 FPGA DSP Platforms
- **Lab 8:** System Generator and Vivado HLS Tool Integration
- **Lab 9:** AXI4-Lite Interface Synthesis

Lab Descriptions

- **Lab 1:** Using the Simulink Software – Learn how to use the toolbox blocks in the Simulink software and design a system. Understand the effect sampling rate.
- **Lab 2:** Getting Started with Xilinx System Generator – Illustrates a DSP48-based design. Perform hardware co-simulation verification targeting a Xilinx evaluation board.
- **Lab 3:** Signal Routing – Design padding and unpadding logic by using signal routing blocks.
- **Lab 4:** Implementing System Control – Design an address generator circuit by using blocks and Mcode.
- **Lab 5:** Designing a MAC-Based FIR – Using a bottom-up approach, design a MAC-based bandpass FIR filter and verify through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 6:** Designing a FIR Filter Using the FIR Compiler Block – Design a bandpass FIR filter by using the FIR Compiler block to demonstrate increased productivity. Verify the design through hardware co-simulation by using a Xilinx evaluation board.
- **Lab 7:** System Generator and Vivado IDE Integration – Embed System Generator models into the Vivado IDE.
- **Lab 8:** System Generator and Vivado HLS Tool Integration – Generate IP from a C-based design to use with System Generator.
- **Lab 9:** AXI4-Lite Interface Synthesis – Package a System Generator for DSP design with an AXI4-Lite interface and integrate this packaged IP into a Zynq All Programmable SoC processor system.

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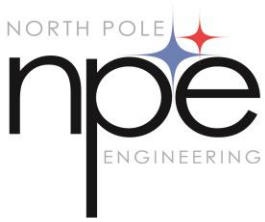

You must have your tuition payment information available when you enroll. We accept credit cards (Visa, MasterCard, or American Express) as well as purchase orders and Xilinx training credits.

Student Cancellation Policy

- Students cancellations received more than 7 days before the first day of class are entitled to a 100% refund. Refunds will be processed within 14 days.
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