

## Course Description

Are you interested in learning how to effectively utilize 7 series architectural resources? This course supports both experienced and less experienced FPGA designers who have already completed the *Essentials of FPGA Design* course. This course focuses on understanding as well as how to properly design for the primary resources found in this popular device family. Topics covered include device overviews, CLB construction, MMCM and PLL clocking resources, global, regional and I/O clocking techniques, memory, FIFO resources, DSP, and source-synchronous resources. Memory controller support and the dedicated hardware resources available in each of the families (PCI Express® technology, analog to digital converters and gigabit transceivers) are also introduced.

This course also includes a detailed discussion about proper HDL coding techniques that enables designers to avoid common mistakes and get the most out of their FPGA. A combination of modules and labs allow for practical hands-on application of the principles taught.

**Level** – FPGA 3

**Course Duration** – 2 days

**Price** – \$1400 or 14 Xilinx Training Credits

**Course Part Number** – 7S-21000-ILT

**Who Should Attend?** – For those who have taken the *Essentials of FPGA Design* course

#### Prerequisites

- *Essentials of FPGA Design* course
- Intermediate VHDL or Verilog knowledge

#### Software Tool

- Vivado® Design or System Edition 2014.1

#### Hardware

- Architecture: Artix®-7, Kintex®-7, and Virtex®-7 FPGAs
- Demo board: None

\* This course focuses on the 7 series FPGA architectures. Check with North Pole Engineering, Inc., for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe all the functionality of the 6-input LUT and the CLB construction of the 7 series FPGAs
- Specify the CLB resources and the available slice configurations for the 7 series FPGAs
- Define the block RAM, FIFO, and DSP resources available for the 7 series FPGAs
- Properly design for the I/O block and SERDES resources
- Identify the MMCM, PLL, and clock routing resources included with these families
- Identify the hard resources available for implementing high performance DDR3 physical layer interfaces
- Describe the additional dedicated hardware for all the 7 series family members
- Properly code your HDL to get the most out of the 7 series FPGAs

## Course Outline

### Day 1

- 7 Series FPGA Overview
- CLB Architecture
- Slice Flip-Flops
- **Lab 1:** CLB Resources
- Memory Resources

- **Lab 2:** Memory Resources
- DSP Resources
- **Lab 3:** DSP Resources

### Day 2

- I/O Resources
- **Lab 4:** I/O Resources
- Clocking Resources
- **Lab 5:** Clocking Resources
- Memory Controllers
- Dedicated Hardware
- Coding Techniques

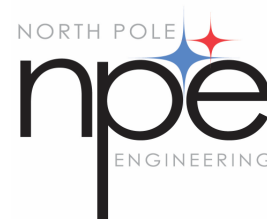
## Lab Descriptions

- **Lab 1: CLB Resources** – Synthesize a 32-bit incrementer with terminal count logic and pipelining registers. Verify that the appropriate resources were used with the Device and Schematic viewers included with the Vivado Design Suite. Use the Schematic Viewer to inspect the implemented results.
- **Lab 2: Memory Resources** – Complete the RTL code required to infer a dual-ported block RAM. Explore the design using the Schematic viewer. As an optional step, change the RTL code to infer a WRITE\_FIRST block RAM.
- **Lab 3: DSP Resources** – Synthesize and implement a 24x17 MAC. Device usage will be verified via the Schematic viewer. As an optional step, using the IP Catalog, construct, instantiate, and implement a wide pipelined multiplier. Verify the results with the Schematic viewer.
- **Lab 4: I/O Resources** – Using the SelectIO Interface Wizard from the IP Catalog, construct a high-speed, clock-forwarded output interface. Explore through simulation the behavior of the various blocks. Also use the Schematic viewer to explore the physical resources of the 7 series FPGA tile used for construction of the high-speed output interface.
- **Lab 5: Clocking Resources** – Using the Clocking Wizard, build and optimize the appropriate MMCM and clock routing resources. Also instantiate these resources into the design. After the design is implemented, verify hardware usage with the Schematic viewer and explore other aspects of the silicon layout.

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