

# WiFi-IT!™

## WLAN Module

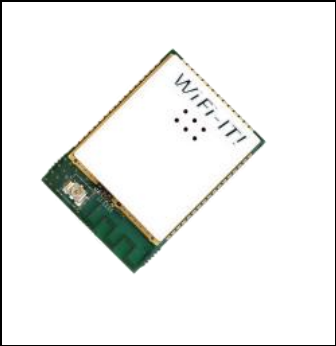
WL11

### WiFi-IT!

#### KEY FEATURES

- FCC/IC/WiFi Certified
- 802.11 b/g/n Compatible
- Dual ARM7 Processors for application and networking
- Small Form Factor (1.28" x 0.9" x 0.143")
- Timer and Event Triggered Auto-reporting Capability
- Analog, Digital, Serial and PWM Interfaces
- Real-Time Clock with Alarm Inputs and Control Outputs
- Security: WEP128, WPA-PSK and WPA2-PSK (TKIP / AES)
- WLAN and TCP/IP Stacks Built-in
- UART Interfaces Support Hardware Flow Control
- 40 to +85 °C Operating Temperature Range
- 3.3 Volt Nominal Operating Voltage

802.11b/g/n  
Wireless  
Network  
Module



#### GENERAL INFORMATION

The WiFi-IT wireless module is a low cost, easy to integrate, robust solution for providing Wi-Fi® connectivity for embedded devices. The WiFi-IT family of modules is perfectly suited for creating a wide variety of wireless applications including sensor-based networks that leverage the existing 802.11 wireless infrastructure. The module combines two ARM7 processors, an RF transceiver, 802.11 MAC, FLASH and SRAM memories with a wide range of interfaces including, two UARTs, two SPI (master and slave), I2C, Digital, Analog and Pulse Width Modulated (PWM) outputs creating a full system on a chip (SoC).

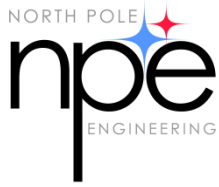
The dual ARM7 architecture with many industry standard interfaces is extremely power efficient and provides a flexibility not found in other 802.11 solutions. The SoC architecture allows one ARM7 to be dedicated to the wireless subsystem. While the other ARM7 can be dedicated to application processing, resulting in a system that can either supplement a standard microprocessor embedded design or totally replace the external microprocessor in the design. This results in lower power consumption, low system requirements and lower total cost. In addition, NPE provides a total programming solution using WiFi-Basic which allows developers to use the WiFi-IT to bring up a Wi-Fi design is as little as a few hours.

The WiFi-IT is available in four pin compatible configurations offering different antenna and power output options.

The WiFi-IT module meets FCC/IC regulatory certification and is fully compliant with EU and R&TTE Directive for Radio Spectrum. It is also pre-scan compliant with Japan Radio Type Approval (i.e. TELEC).

## FEATURES

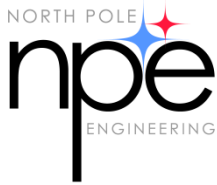
- ❖ Family of modules providing different antenna and output power options:
  - Available with internal or external power amplifier
  - Two module package sizes
  - Fully pin compatible
  - PCB antenna / External antenna connector
- ❖ Two general-purpose SPI interfaces
  - Configurable as either master or slave
  - One interface provides integrated chip-select lines
- ❖ Two multi-purpose UART interfaces
  - Standard bit rates up to 921.6 kbps
  - RTS/CTS flow control
  - 5,6,7 and 8-bit character formats
  - 1 or 2 stop bits (1.5 in case of a 5-bit character format)
  - Parity bit: none, even, odd, mark or space
  - 16-byte transmit and receive FIFOs
- ❖ I<sup>2</sup>C master/slave interface
  - 100 Kbps standard mode operation
  - 392 Kbps fast speed mode operation
  - 7 or 10-bit addressing
  - Digital debounce logic for the received SDA and SCL lines
  - Hold Delay insertion on SDA line
- ❖ PWM output
- ❖ Up to 23 configurable general purpose I/Os
  - Configurable pull up / pull down
  - Two high-drive outputs (up to 20 mA)
- ❖ Two ADC channels
  - aggregate sample rate 32 kSps
- ❖ Two alarm inputs, asynchronously wake-up chip
- ❖ Embedded Real Time Clock (RTC)
  - Can run directly from battery



## WiFi-IT!™ WLAN Module

WL11

- ❖ Power supply monitoring capability
- ❖ Low-power modes
  - Sleep, deep sleep and standby



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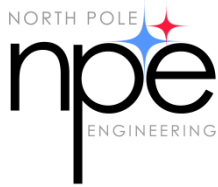
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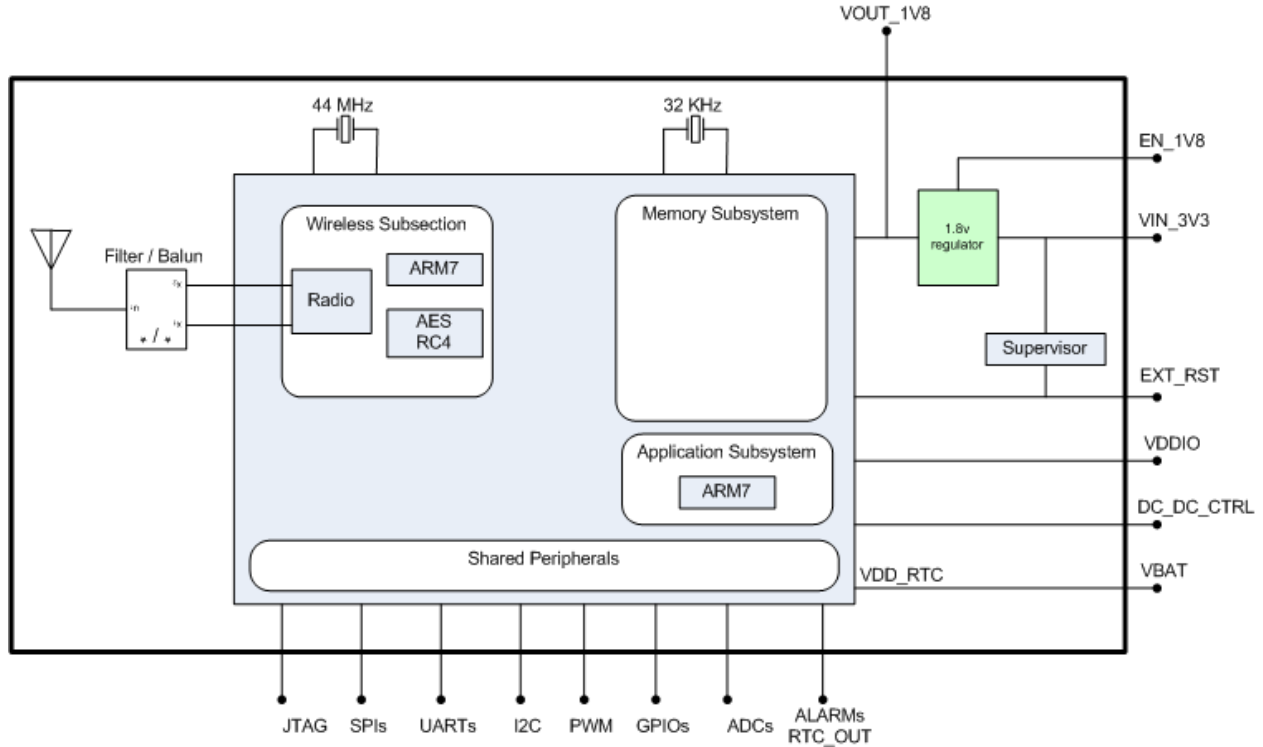


WiFi-IT!™  
WLAN Module

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**MODULE BLOCK DIAGRAM**



**HARDWARE DESCRIPTION**

The WiFi-IT is a highly integrated, ultra low power module that contains a Media Access Controller (MAC), WLAN PHY and baseband functionality, two ARM7 processors, on-chip FLASH and SRAM memories and a number of industry standard interfaces. The module family uses a single power supply with optional module controlled external regulator enable control pin (DC\_DC\_CTRL). An RTC (Real Time Clock) with battery supply monitor option (VBAT) and a control output (RTC\_OUT) can wake the module and the remainder of the system periodically.

**WIRELESS SUBSECTION**

The wireless subsection is controlled by the WLAN CPU, this is a 32-bit ARM7 TDMI-S core running at up to 44 MHz. It includes the IEEE 802.11 b/g/n compatible RF transceiver, which supports Direct Sequence Spread Spectrum (DSSS) at 1 and 2 Mbps data rates and Complementary Code Keyed (CCK) operation at 5.5 and 11 Mbps data rates. The WLAN subsection includes an integrated power amplifier and provides management capabilities for an optional external power amplifier. This section also contains support for AES-CCMP and RC4 encryption/decryption.

#### **MEMORY SUBSECTION**

There are several memory blocks in the WiFi-IT! module. The Boot ROM block (60 kB) provides the capability to download new firmware via the SPI Slave or UART0 interfaces and to control the update of the WLAN and APP FLASH memories.

The embedded FLASH memory is implemented as three 128 KB FLASH blocks. The three FLASH blocks are dedicated to the WLAN, APP0 and APP1. The WLAN FLASH contains the WLAN firmware. the APP 0 and 1 FLASH memories contain the network and application software.

#### **DC\_DC\_CTRL**

During power on reset the DC\_DC\_CTRL pin is held low. It goes high to indicate completion of the Real-Time Clock (RTC) power on reset. This pin is generally used to enable as an enable to an external voltage regulator.

#### **ALARM INPUTS 1/2**

There are two inputs to the RTC, Alarm1 and Alarm2. The Alarm inputs have programmable polarity with Schmidt-triggered logic. They are used to wake-up the system from the power conservation sleep modes, when an external event occurs, by setting DC\_DC\_CTRL high. A GPIO can be used as a Ready output which goes active when the module is ready to communicate.

#### **REAL TIME CLOCK (RTC)**

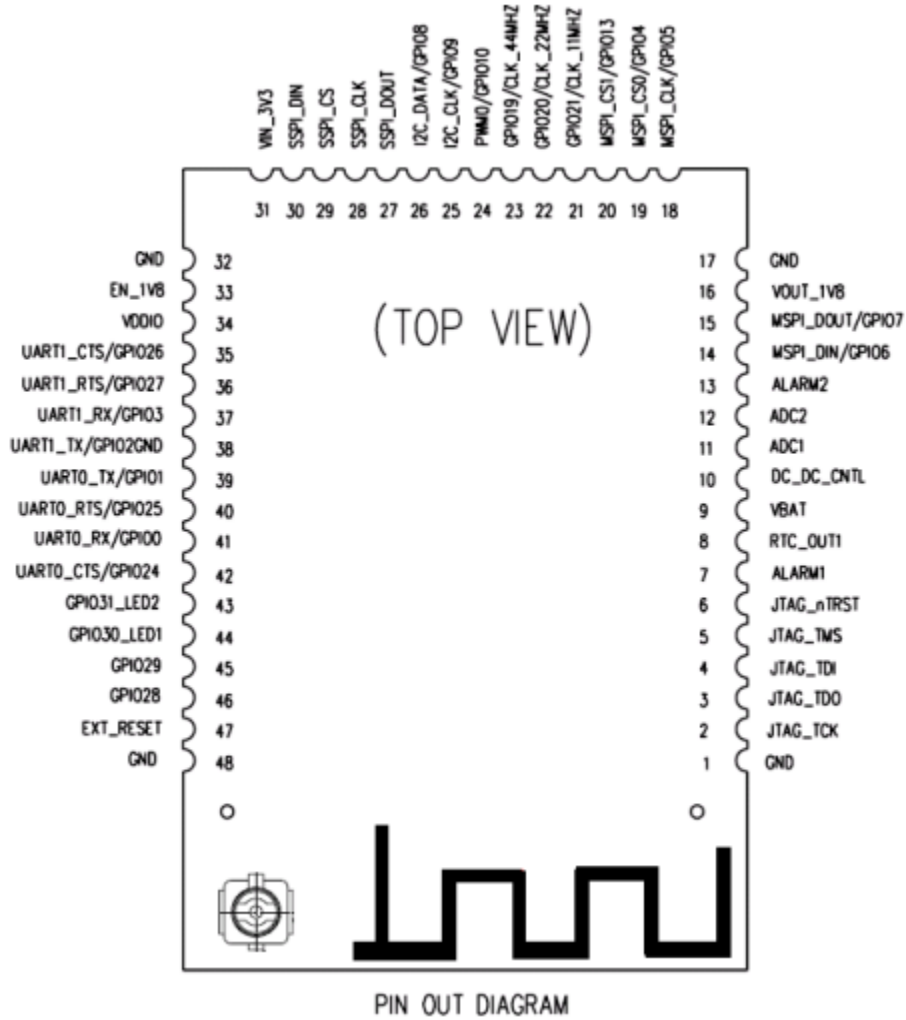
The RTC provides global time and date to the system. The RTC includes 128x32 battery-backed SRAM and a real time counter (48-bits; 46-bits effective). The RTC is driven by a 32.768 kHz crystal, which is part of the module. In normal operation the RTC is always powered, allowing it to provide periodic interrupts to wake the system from any of the low-power modes.

Total current consumption of the RTC, worst case, is typically less than 5 uA without data storage.

#### **RTC\_OUT1**

The RTC\_OUT1 signal can be disabled or driven by wake-up counter 2. This is a 34-bit counter. The RTC-OUT1 signal can be configured to output the low-power crystal oscillator clock (32.768 kHz) or a simple state transition that can be used to enable external circuitry.

**PIN-OUT AND SIGNAL DESCRIPTION**



The following table lists the WL11 module signals. For I/O signals that share functionality with GPIO pins, the default functional state after reset is GPIO, with pins configured as inputs. The bias column indicates the value of the default internal bias after a hardware reset.

PIN	SIGNAL	ALTERNATE	I/O	DESCRIPTION	BIAS	DRIVE
1	GND	—	—	Ground	—	—
2	TCK <sup>1</sup>	—	I	JTAG Clock Input	PU	—
3	TDO	—	O	JTAG Data Output		4 ma
4	TDI <sup>1</sup>	—	I	JTAG Data Input	PU	—

PIN	SIGNAL	ALTERNATE	I/O	DESCRIPTION	BIAS	DRIVE
5	TMS <sup>1</sup>	—	I	JTAG Control Input	PU	—
6	TRSTn <sup>1</sup>	—	I	JTAG Active Low Reset Input	PU	—
7	ALARM1 <sup>1</sup>	—	I	RTC Wake-Up Input 1	PU	—
8	RTC_OUT1	—	O	Sensor Wake Real-Time Clock Output 1	—	4 ma
9	VBAT	—	I	Embedded Real Time Clock Power Supply	—	—
10	DC_DC_CTRL	—	O	VIN_3V3 Regulator Control Output	—	4 ma
11	ADC1 <sup>5</sup>	DAC	I/O	ADC Channel 1 Input / DAC Output	—	—
12	ADC2 <sup>5</sup>	VREF	I	ADC Channel 2 Input / Analog Reference Voltage Input	—	—
13	ALARM2 <sup>1</sup>	—	I	RTC Wake-Up Input 2	PD	—
14	MSPI_DIN	GPIO_06	I/O	SPI Master Data Input	PD	4 ma
15	MSPI_DOUT	GPIO_07	I/O	SPI Master Data Input	PD	4 ma
16	VOUT_1V8	—	O	Internal 1.8 volt output	—	?
17	GND	—	—	Ground	—	—
18	MSPI_CLK	GPIO_05	I/O	SPI Master Clock Output	PD	4 ma
19	MSPI_CS0	GPIO_04	I/O	SPI Master Chip Select 0 Output	PD	4 ma
20	MSPI_CS1	GPIO_13	I/O	SPI Master Chip Select 1 Output	PD	4 ma
21	CLK_11MHz	GPIO_21	I/O	11 MHz Clock Output Test Point	PD	4 ma
22	CLK_22MHz	GPIO_20	I/O	22 MHz Clock Output Test Point	PD	4 ma
23	CLK_44MHz	GPIO_19	I/O	44 MHz Clock Output Test Point	PD	4 ma
24	PWM0	GPIO_10	I/O	Pulse Width Modulated Output 0	PD	4 ma
25	I2C_CLK <sup>4</sup>	GPIO_09	I/O	I2C Clock	PD	12 ma
26	I2C_DATA <sup>4</sup>	GPIO_08	I/O	I2C Data	PD	12 ma
27	SSPI_DOUT <sup>1</sup>	—	I/O	SPI Slave Data Output	PU	4 ma
28	SSPI_CLK <sup>1</sup>	—	I	SPI Slave Clock Input	PU	4 ma
29	SSPI_CS <sup>1</sup>	—	I	SPI Slave Chip Select Input	PU	4 ma
30	SSPI_DIN <sup>1</sup>	—	I	SPI Slave Data Input	PD	4 ma
31	VIN_3V3	—	I	3.3 volt power	—	—
32	GND	—	—	Ground	—	—

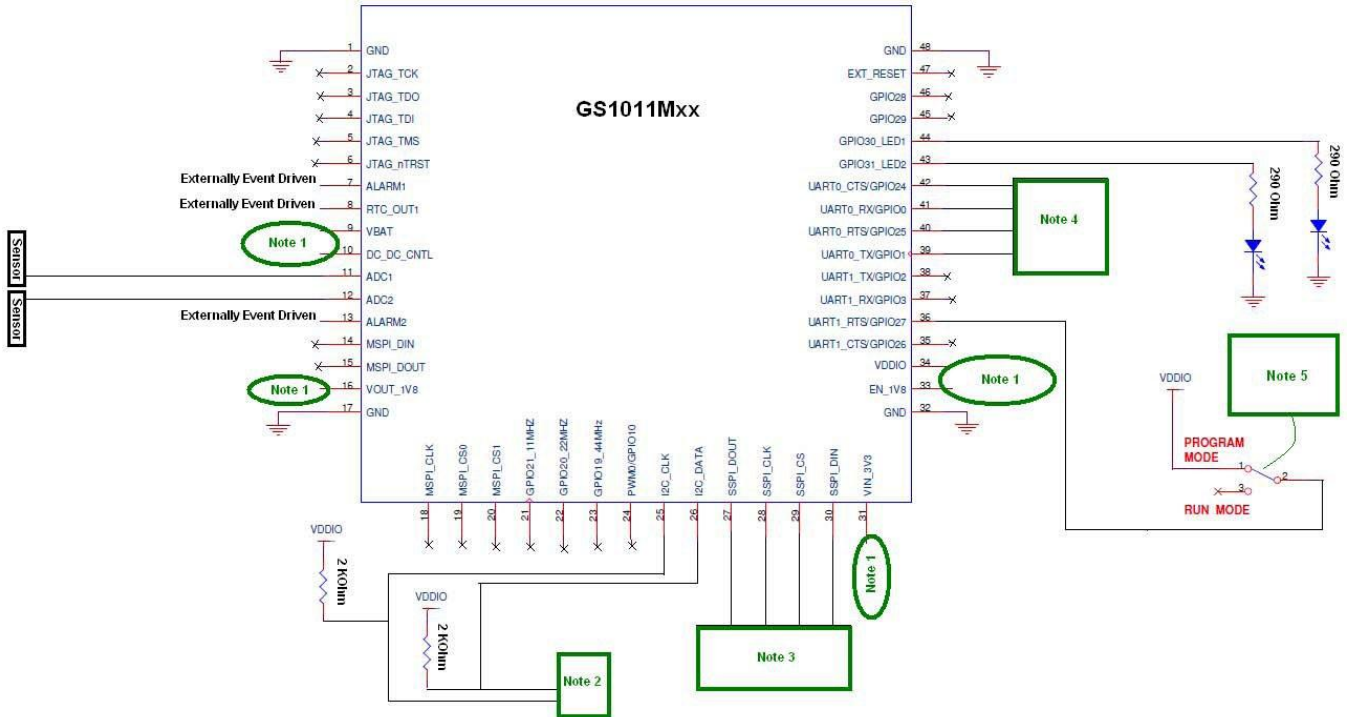
PIN	SIGNAL	ALTERNATE	I/O	DESCRIPTION	BIAS	DRIVE
33	EN_1V8 <sup>5</sup>	—	I	Internal 1.8v Regulator Enable (active high)	—	—
34	VDDIO	—	I	I/O voltage domain	—	—
35	UART1_CTS	GPIO_26	I/O	UART 1 Clear to Send Input	PD	4 ma
36	UART1_RTS <sup>2</sup>	GPIO_27	I/O	UART 1 Request to Send Output	PD	4 ma
37	UART1_RX	GPIO_03	I/O	UART 1 Receive Data Input	PD	4 ma
38	UART1_TX	GPIO_02	I/O	UART 1 Transmit Data Output	PD	4 ma
39	UART0_TX	GPIO_01	I/O	UART 0 Transmit Data Output	PD	4 ma
40	UART0_RTS <sup>6</sup>	GPIO_25	I/O	UART 0 Request to Send Output \ WiFi-Basic Boot Loader	PD	4 ma
41	UART0_RX	GPIO_00	I/O	UART 0 Receive Data Input	PD	4 ma
42	UART0_CTS	GPIO_24	I/O	UART 0 Clear to Send Input	PD	4 ma
43	LED1	GPIO_31	I/O	High Drive Output 1	PD	20 ma
44	LED0	GPIO_30	I/O	High Drive Output 0	PD	20 ma
45	CFG1 <sup>3</sup>	GPIO_29	I/O	JTAG Configuration 1 Input	PD	4 ma
46	CFG0 <sup>3</sup>	GPIO_28	I/O	JTAG Configuration 0 Input	PD	4 ma
47	EXT_RESETn	—	I/O	External Reset Output / Module Reset Input	—	—
48	GND	—	I	Ground	—	—

**Table 1: Interface Signal Description**

**NOTES**

1. THESE PINS HAVE ONBOARD HARDWARE CONFIGURED PULL-UPS/DOWNS AND CANNOT BE CHANGED BY SOFTWARE.
2. IF UART1\_RTS IS HIGH DURING BOOT, THEN THE WLAN WILL WAIT FOR FLASH DOWNLOAD VIA UART0. FOR DEVELOPMENT PURPOSES, ROUTE THIS PIN TO A TEST POINT ON THE BOARD SO IT CAN BE PULLED UP TO VIN\_3V3.
3. GPIO 28 AND 29 ARE SAMPLED AT RESET TO ESTABLISH JTAG CONFIGURATION FOR DEBUGGING. THESE SIGNALS SHOULD NOT BE DRIVEN FROM AN EXTERNAL DEVICE. IF USING JTAG, CONFIGURE THESE PINS AS OUTPUTS.
4. IF I2C INTERFACE IS USED, PROVIDE 2K OHM PULL-UPS, TO VDDIO, FOR PINS 25 AND 26 (I2C\_CLK AND I2C\_DATA).
5. EN\_1V8 NEEDS TO BE DRIVEN HIGH OR LOW EXTERNALLY. THIS SIGNAL IS ACTIVE HIGH.
6. IF UART0\_RTS/GPIO\_25 IS HIGH DURING BOOT, THEN THE WiFi-BASIC BOOT LOADER WILL BE ACTIVE – THE WiFi-BASIC PROGRAM WILL NOT RUN, AND WILL WAIT TO LOAD A NEW WiFi-BASIC PROGRAM THROUGH UART0.

**GENERAL CONNECTION DIAGRAM**



**Module pin connection diagram**

Note 1: For the noted pin configurations, please refer to data sheet power supply section.

Note 2: If I2C interface is used, provide 2K ohm pull-ups, to VDDIO, for pins 25 and 26 (I2C\_CLK and I2C\_DATA). If not used, leave pins 25 and 26 unconnected.

Note 3: Connect to external HOST SPI (can be left unconnected if not used).

Note 4: Connect to external serial HOST UART (can be left unconnected if not used)

Note 5: This switch enables the programming of GS1011 onboard flash. A switch is recommended for development purposes and is not needed for production.

**TYPICAL POWER SUPPLY CONNECTION DIAGRAMS**

This section details the power supply connections for various types of applications. Certain power supply configurations have some connection differences when using the internal Power Amplifier (PA) modules (WL11-IPx and WL11-IEx) versus the external PA modules (WL11-EPx and WL11-EEx).

**ALWAYS ON POWER SUPPLY CONFIGURATION**

This configuration is common to both types of modules, internal and external PA. It targets designs that use 3.3v IO and is always powered on.

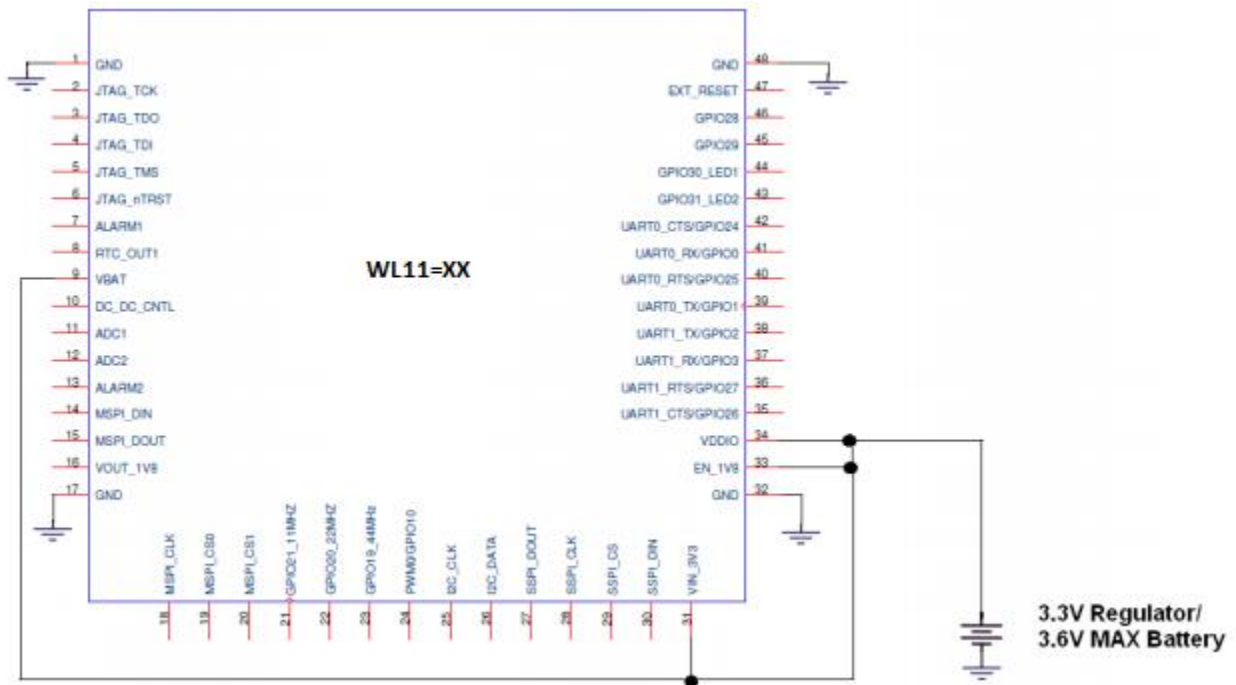


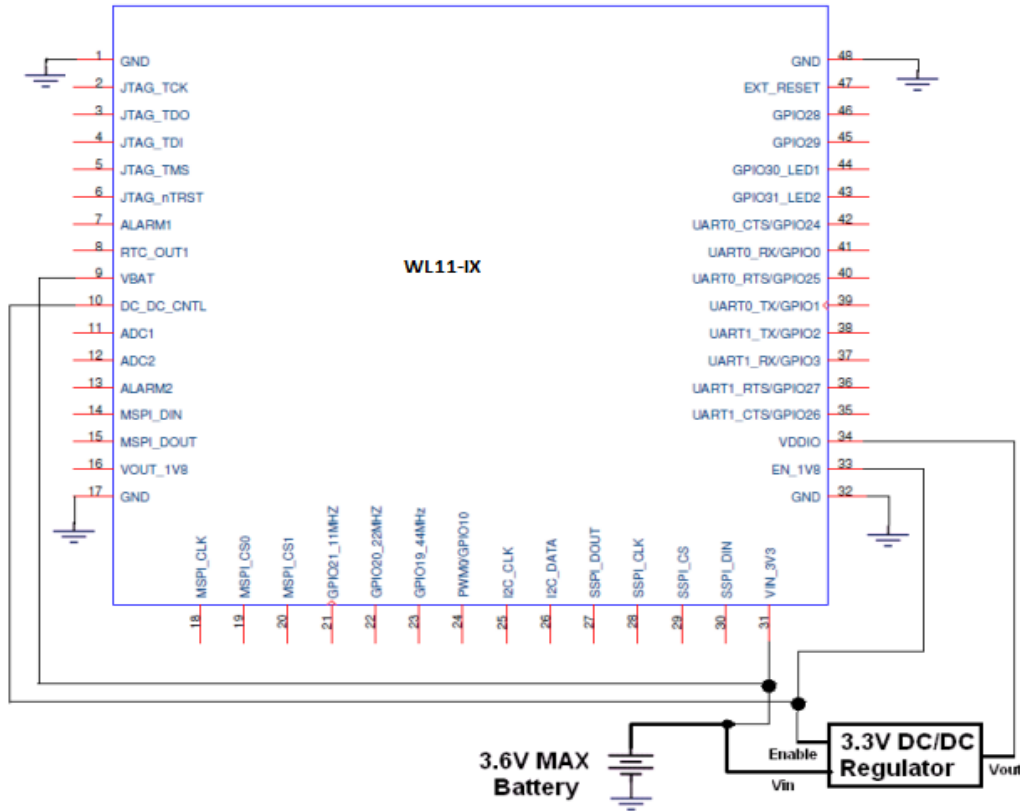
Figure 1: Always On Power Supply Configuration

**DESIGN NOTES:**

1. The always on power condition is obtained by tying EN\_1V8 high, which enables the 1.8v regulator that powers the core voltages.
2. This power configuration allows the module to go into the deep sleep state to take advantage of low power consumption, but the system will not go into the lowest power state – standby.

**INTERNAL PA, BATTERY POWERED WITH 3.3V IO AND STANDBY SUPPORT**

This design configuration should be used for internal PA designs that will be utilizing standby (the lowest power state) and that are generally battery powered.



**Figure 2: Internal PA, Battery Powered, 3.3v IO with Standby Support**

**DESIGN NOTES:**

1. VIN\_3V3 is always powered to take advantage of the low latency wake up time (< 15 mS) from standby.
2. VDDIO should be powered down when the module is in Standby. It is recommended to use DC\_DC\_CTRL to control VDDIO along with EN\_1V8, which controls the core 1.8 volt regulator. DC\_DC\_CTRL will be de-asserted when the system goes into Standby.
3. VBAT must always be powered to retain functionality of the Real Time Clock (RTC) and associated logic.

**INTERNAL PA, BATTERY POWERED WITH 1.8V IO AND STANDBY SUPPORT**

This design configuration should be used for internal PA designs that will be utilizing standby (the lowest power state) and that are generally battery powered but use 1.8v for all IO.

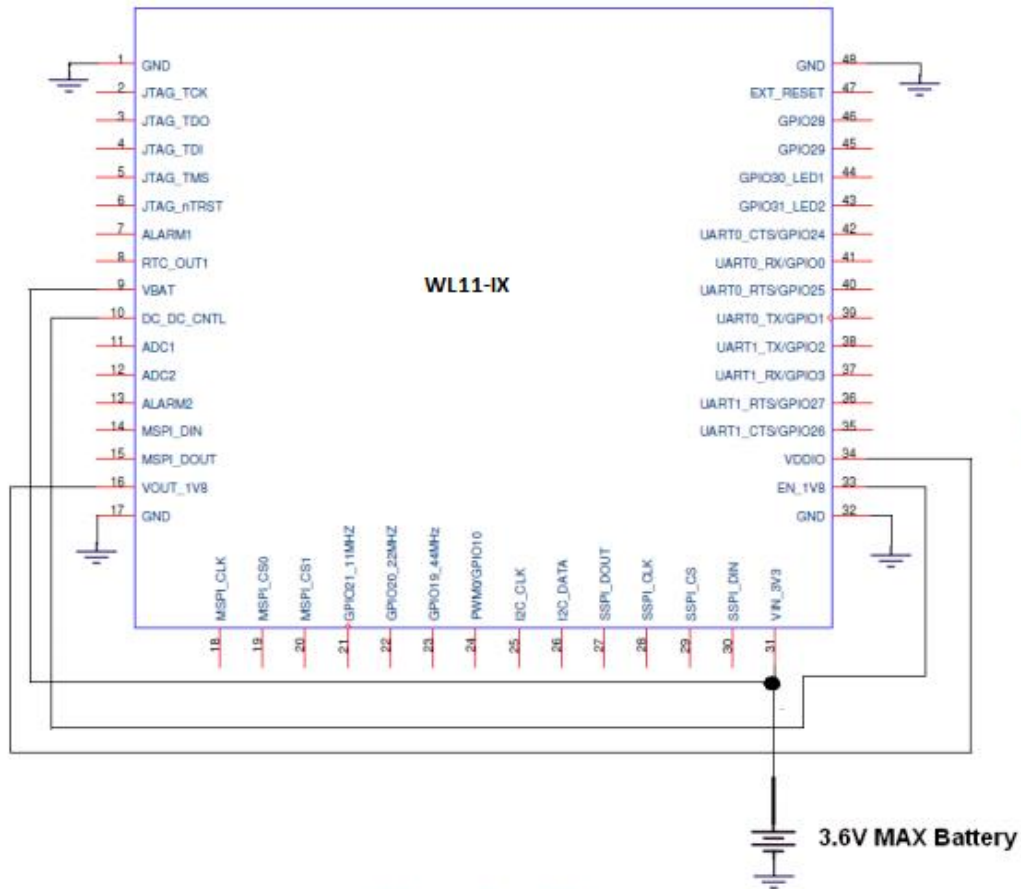


Figure 3: Internal PA, Battery Powered, 1.8v IO with Standby Support

**DESIGN NOTES:**

1. DC\_DC\_CTRL should be tied to EN\_1V8 to turn off the internal 1.8v core voltage regulator when the device enters Standby. This keeps current consumption to a minimum.

**EXTERNAL PA, BATTERY POWERED WITH 3.3V IO AND STANDBY SUPPORT**

This design is for external PA designs, running on battery power, that require Standby to take advantage of the lowest power consumption.

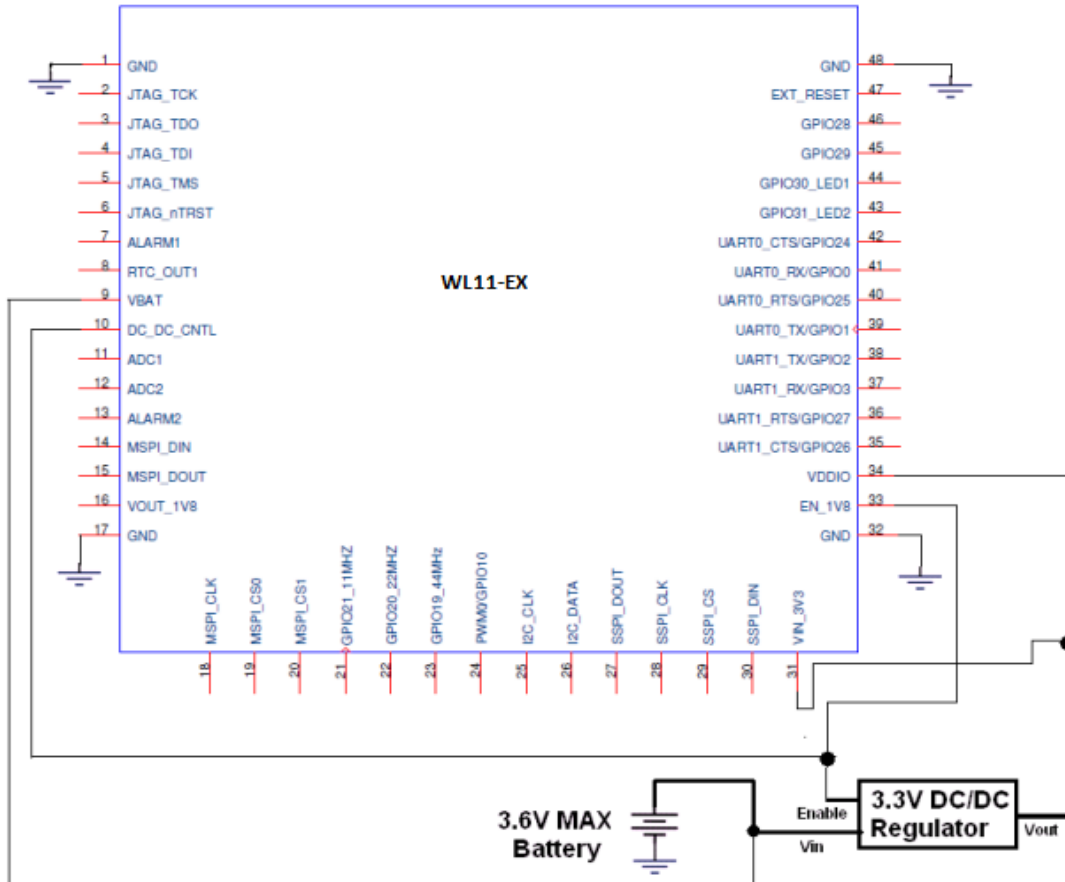


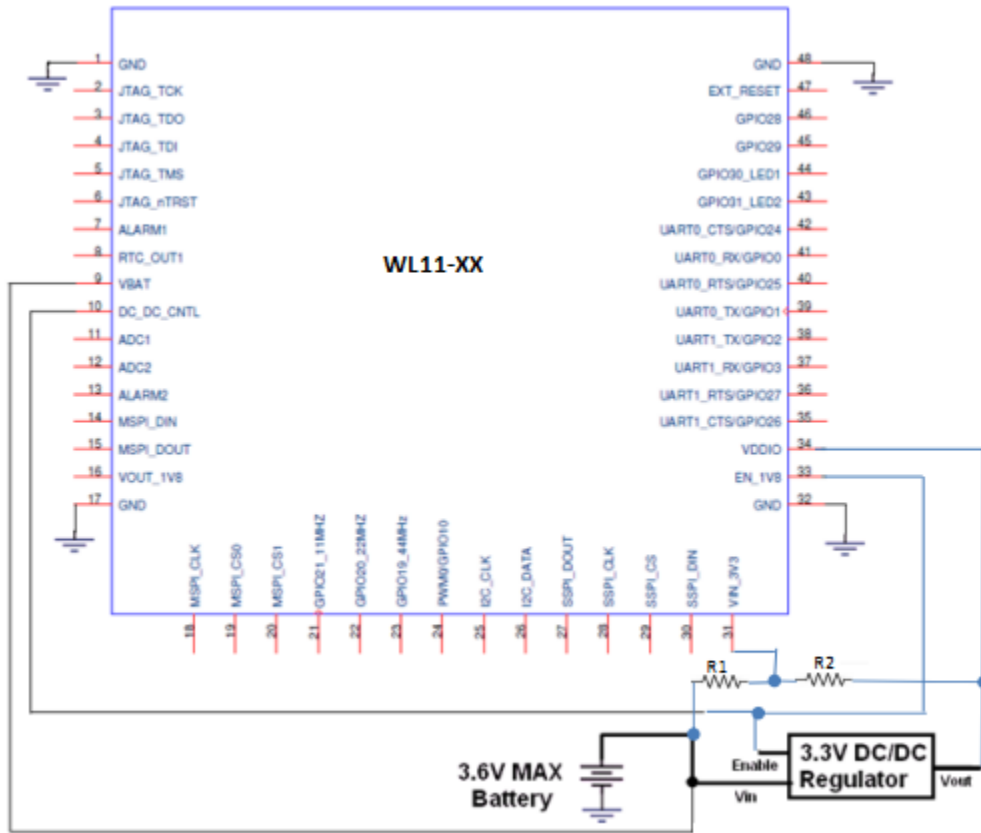
Figure 4: External PA, Battery Powered, 3.3v IO with Standby Support

**DESIGN NOTES:**

1. The external PA is supplied with power through VIN\_3V3. In rush currents required by the external PA require the DC/DC regulator be a buck/boost type depending on the battery used.
2. VDDIO and VIN\_3V3 power must be shut off in standby mode so there is no leakage from the external PA to achieve the lowest power savings.
3. Since power to VIN\_3V3 is removed in this configuration the device will be held in reset until the internal voltage supervisor releases the reset signal.

**DUAL MODULE DESIGNS USING STANDBY**

Using the same design with either the internal or external PA modules can provide flexibility and save cost. For designs that would like to support either module type and retain the advantages of Standby power savings, this design prototype should be used.



**Dual Module Design with 3.3v IO and Standby Support**

**DESIGN NOTES:**

- Resistors R1 and R2 are stuffing options that depend on the module type (IP/EP) used.

MODULE TYPE	STUFFING OPTION
WL11-Ixx	R1 ONLY
WL11-Exx	R2 ONLY

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

CONDITIONS BEYOND THOSE CITED IN TABLE A-1 MAY CAUSE PERMANENT DAMAGE TO THE WL11XX, AND MUST BE AVOIDED.

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
STORAGE TEMPERATURE	TST	-55		+125	°C
RTC POWER SUPPLY	VBAT	-.05		4.0	V
I/O SUPPLY VOLTAGE	VDDIO	-.05		4.0	V
SINGLE SUPPLY PORT	VIN_3V3	2.7	3.3	4.0	V

NOTE: FOR LIMITATIONS ON STATE VOLTAGE RANGES, PLEASE CONSULT SECTION X: POWER SUPPLY

### OPERATING CONDITIONS

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT
EXTENDED TEMP. RANGE	TA	-40		+85	°C
RTC POWER SUPPLY	VBAT	1.2		3.6	V
I/O SUPPLY VOLTAGE	VDDIO	1.7		3.6	V
SINGLE SUPPLY PORT WL11X (AS CONFIGURED PER FIGURE 1, 2 & 3)	VIN_3V3	2.7	3.3	3.6	V
SINGLE SUPPLY PORT WL11X (AS CONFIGURED PER FIGURE 4)	VIN_3V3	3.0	3.3	3.6	V

### INTERNAL 1.8V REGULATOR

VIN\_3V3=VDDIO=VBAT=3.3V TEMP=25°C FOSC=3.0MHZ

PARAMETER	SYMBOL	TEST CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNIT
OUTPUT VOLTAGE	VOUT_1V8			1.8		V
MAXIMUM OUTPUT CURRENT	IVOUT_1V8			30	50	MA
OSCILLATION FREQUENCY	Fosc		1.6		3.45	MHZ
1.8V REGULATOR ENABLE "H" VOLTAGE	EN_1V8		1.0		VIN_3V3	V
1.8V REGULATOR ENABLE "H" VOLTAGE	EN_1V8		1.0		VIN_3V3	V

**I/O DC SPECIFICATIONS**

**DIGITAL INPUT SPECIFICATIONS**

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
INPUT LOW VOLTAGE	V <sub>IL</sub>	-0.3		0.25*VDD <sub>IO</sub>	V	
INPUT HIGH VOLTAGE	V <sub>IH</sub>	0.8*VDDIO		VDDIO	V	

**DIGITAL OUTPUT SPECIFICATIONS**

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
OUTPUT LOW VOLTAGE	V <sub>OL</sub>	-0.3		0.25*VDD <sub>IO</sub>	V	
OUTPUT HIGH VOLTAGE	V <sub>OH</sub>	0.8*VDDIO		VDDIO	V	
OUTPUT RISE TIME @ VDDIO=3.3V	T <sub>TLH</sub>			7	NS	WITH 4 MA, 33 PF LOAD
OUTPUT RISE TIME @ VDDIO=3.3V	T <sub>TLH</sub>			7	NS	WITH 4 MA, 33 PF LOAD

**I/O DIGITAL SPECIFICATIONS (TRI-STATE)**

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
INPUT LOW VOLTAGE	V <sub>IL</sub>	-0.3		0.25*VDD <sub>IO</sub>	V	
INPUT HIGH VOLTAGE	V <sub>IH</sub>	0.8*VDD <sub>IO</sub>		VDDIO	V	
SCHMITT TRIG. LOW TO HIGH THRESHOLD POINT	V <sub>T+</sub>	1.5			V	
SCHMITT TRIG. HIGH TO LOW THRESHOLD POINT	V <sub>T-</sub>	1.5			V	
INPUT LEAKAGE CURRENT	I <sub>L</sub>			5	uA	PULL UP/DOWN DISABLED
TRI-STATE OUTPUT LEAKAGE CURRENT	O <sub>ZL</sub>			5	uA	PULL UP/DOWN DISABLED
PULL-UP RESISTOR	R <sub>U</sub>	0.05		1	MΩ	
PULL-DOWN RESISTOR	R <sub>D</sub>	0.05		1	MΩ	
OUTPUT LOW VOLTAGE	V <sub>OL</sub>	0		0.4	V	WITH 4/12/20 MA LOAD
OUTPUT HIGH VOLTAGE	V <sub>OH</sub>	1.3 V		VDDIO	V	WITH 4/12/20 MA LOAD WITH 2/6/10 MA LOAD

OUTPUT RISE TIME@ VDDIO=3.3V	TTOLH			7	NS	WITH 4/12/20 MA LOAD 33 PF
OUTPUT FALL TIME@ VDDIO=3.3V	TTOHL			7	NS	WITH 4/12/20 MA LOAD, 33 PF
INPUT RISE TIME	TTILH			7	NS	
INPUT FALL TIME	TTIHL			7	NS	

### RTC INPUT SPECIFICATIONS (WITH SCHMITT TRIGGER)

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
I/O SUPPLY VOLTAGE	VDDRTC	1.2		VBAT	V	
INPUT LOW VOLTAGE	VIL	-0.3		0.25*VDDRTC	V	
INPUT HIGH VOLTAGE	VIH	0.8*VDDRTC		VDDRTC	V	
SCHMITT TRIG. LOW TO HIGH THRESHOLD POINT	Vt+	0.57*VDDRTC		0.68*VDDRTC	V	
SCHMITT TRIG. HIGH TO LOW THRESHOLD POINT	Vt-	0.27*VDDRTC		0.35*VDDRTC	V	
INPUT LEAKAGE CURRENT	IL		260		PA	

### RTC OUTPUT SPECIFICATIONS

PARAMETER	SYMBOL	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
I/O SUPPLY VOLTAGE	VDDRTC	1.2		VBAT	V	
OUTPUT LOW VOLTAGE	VOL			0.4	V	
OUTPUT HIGH VOLTAGE	VOH	0.8*VDDRTC		VDDRTC	V	
OUTPUT RISE TIME	TTLH	19		142	NS	50 PF LOAD
OUTPUT FALL TIME	TTHL	21		195	NS	50 PF LOAD
INPUT LEAKAGE CURRENT	IL		730		PA	

### POWER CONSUMPTION

SYSTEM STATE	CURRENT (TYP.)
Standby	7 uA
Deep Sleep	110 uA
Receive (WL11xx; -81 dBm RX sens. @ 11 Mb/Sec.)	140 mA
Transmit (WL11lx; +8 dBm at antenna port @ 11 Mb/Sec.)	150 mA
Transmit (WL11MEx; +18 dBm at antenna port @ 11 Mb/Sec.)	250 mA

### RADIO PARAMETERS

TEST CONDITIONS: VDD33=VDDIO=VBAT=3.3V TEMP=25°C

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
RF FREQUENCY RANGE	2412		2497	MHZ	
RADIO BIT RATE	1		11	MBPS	
<b>TRANSMIT SPECIFICATIONS FOR WL11IX</b>					
OUTPUT POWER (AVG)		8		DBM	MODULATED SIGNAL AT ANTENNA PORT; 1 Mb/SEC.
SPECTRUM MASK				DBR	MODULATED SIGNAL AT ANTENNA PORT
F0+/- 11MHZ	-30				
OFFSET >=22 MHZ	-50				
RECEIVE SENSITIVITY AT ANTENNA PORT		-81 -84 -88 -90		DBM	11 MBPS QPSK, 9% PER 5.5 MBPS QPSK, 9% PER 2 MBPS QPSK, 9% PER 1 MBPS QPSK, 9% PER
<b>TRANSMIT SPECIFICATIONS FOR WL11EX</b>					
OUTPUT POWER (AVG)		18		DBM	MODULATED SIGNAL AT ANTENNA PORT; 1 Mb/SEC.
SPECTRUM MASK				DBR	MODULATED SIGNAL AT ANTENNA PORT
F0+/- 11MHZ	-30				
OFFSET >=22 MHZ	-50				
RECEIVE SENSITIVITY AT ANTENNA PORT		-81 -84 -88 -90		DBM	11 MBPS QPSK, 9% PER 5.5 MBPS QPSK, 9% PER 2 MBPS QPSK, 9% PER 1 MBPS QPSK, 9% PER

### ADC PARAMETERS

PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
ADC RESOLUTION	-	10	-	BITS	
ADC SAMPLE FREQ	1.024	-	31.25	KSPS	
ADC INPUT CLOCK FREQ	32.768	-	1000	KHZ	
ADC FULL SCALE VOLTAGE		VOUT_1 V8- 0.036		V	REFERENCE = VOUT_1V8
CONVERSION TIME		32		CLOCKS	BASED ON INTERNALLY GENERATED 1MHZ OR 32.768 KHZ CLOCKS
ADC INTEGRAL NON-LINEARITY (INL)	-2.0	-	2.0	LSB	
ADC DIFFERENTIAL NONLINEARITY (DNL)	-1.0	-	1.0	LSB	

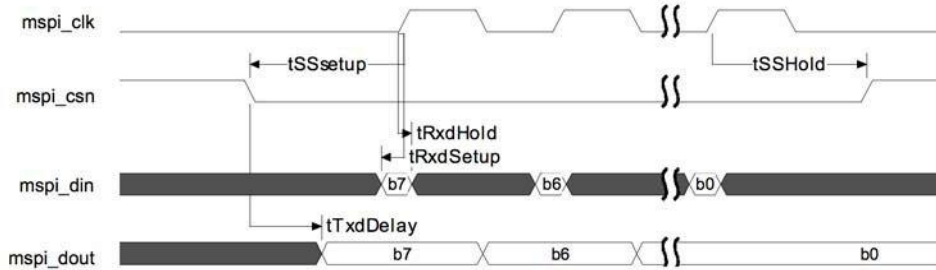
PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT	NOTE
AVDD POWER SUPPLY CURRENT (OPERATIONAL)	-	400	800	UA	
ADC OFFSET ERROR	-10	-	10	mV	
ADC GAIN ERROR	-10	-	10	mV	
SETTLING TIME		-	1	uS	
INPUT RESISTANCE	1	-	-	MOHM	
INPUT CAPACITANCE	-	10	-	PF	
BANDGAP OUTPUT VOLTAGE (VREF) (T=25°C)	1.179	1.24	1.301	V	

**SPI INTERFACE TIMING**

TEST CONDITIONS: VIN\_3V3=VDDIO=VBAT=3.3V TEMP=25°C

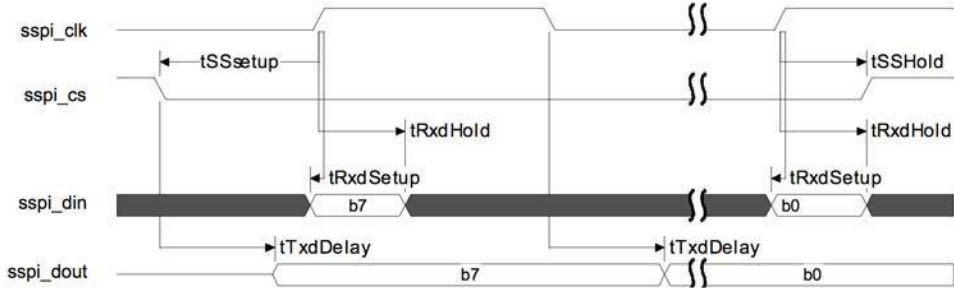
**H-1. MOTOROLA SPI, CLOCK POLARITY SPO = 0, CLOCK PHASE SPH = 0**

**TIMING DIAGRAM, MASTER MODE, SPO=SPH=0**



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST RISING EDGE OF SPI CLOCK	1		MSPI CLOCK PERIOD
TTXDDELAY	DELAY IN MASTER ASSERTING TX LINE AFTER FALLING EDGE OF SELECT LINE		2 CORE SPI CLOCK PERIODS +3 NSEC	MIXED
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	30		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	10		NSEC
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	1		MSPI CLOCK PERIOD

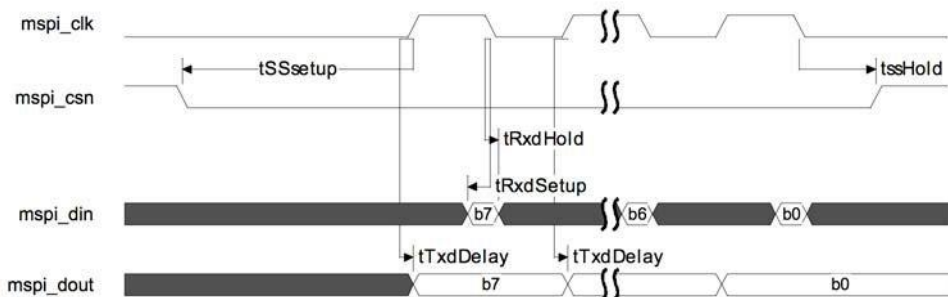
**TIMING DIAGRAM, SLAVE MODE, SPO=SPH=0**



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST RISING EDGE OF SPI CLOCK	4 CORE SPI CLOCK PERIODS +68 NSEC		MIXED
TTXDDelay	DELAY IN SLAVE ASSERTING TX LINE AFTER FALLING EDGE OF SPI CLOCK, OR THE FIRST BIT AFTER FALLING EDGE OF THE SELECT LINE		4 CORE SPI CLOCK PERIODS +68 NSEC	MIXED
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	15		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	3 CORE SPI CLOCK PERIODS +14 NSEC		MIXED
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	3 CORE SPI CLOCK PERIODS +14 NSEC		MIXED

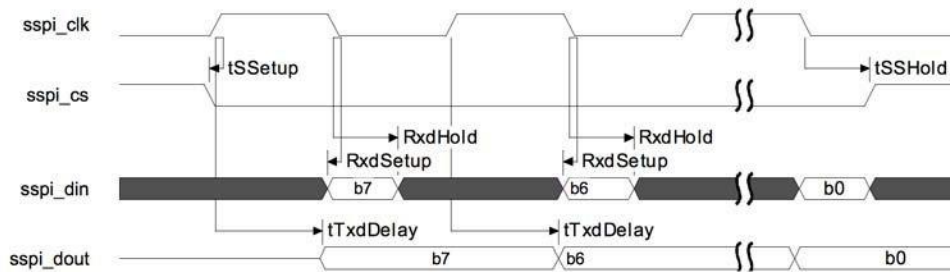
**H-2. MOTOROLA SPI, CLOCK POLARITY SPO = 0, CLOCK PHASE SPH = 1**

**TIMING DIAGRAM, MASTER MODE, SPO=0, SPH=1**



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST RISING EDGE OF SPI CLOCK	1.5		MSPI CLOCK PERIOD
TTXDDELAY	DELAY IN MASTER ASSERTING TX LINE AFTER RISING EDGE OF SPI CLOCK		0	NSEC
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	30		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	10		NSEC
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	0.5		MSPI CLOCK PERIOD

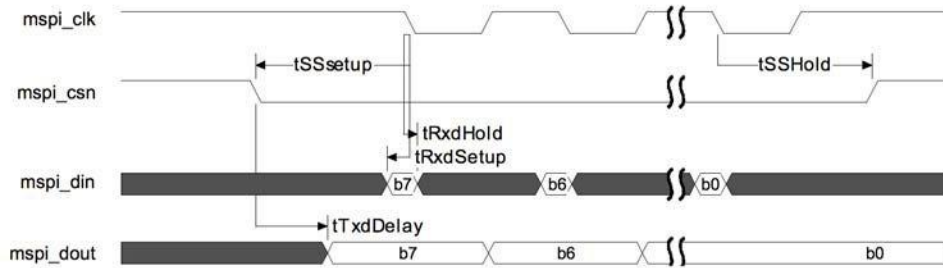
**TIMING DIAGRAM, SLAVE MODE, SPO=0, SPH=1**



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST RISING EDGE OF SPI CLOCK	15		NSEC
TTXDDELAY	DELAY IN SLAVE ASSERTING TX LINE AFTER FALLING EDGE OF SPI CLOCK		4 CORE SPI CLOCK PERIODS + 68 NSEC	MIXED
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	15		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	3 CORE SPI CLOCK PERIODS + 14 NSEC		MIXED
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	3 CORE SPI CLOCK PERIODS + 14 NSEC		MIXED

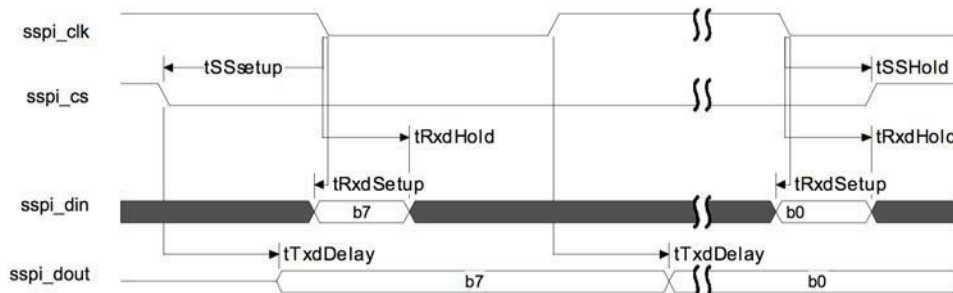
**H-3. MOTOROLA SPI, CLOCK POLARITY SPO = 1, CLOCK PHASE SPH = 0**

**TIMING DIAGRAM, MASTER MODE, SPO=1, SPH=0**



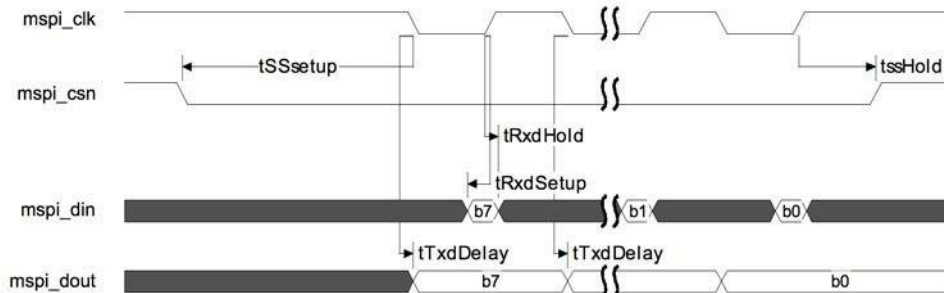
PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST RISING EDGE OF SPI CLOCK	1		MSPI CLOCK PERIOD
TTXDDELAY	DELAY IN MASTER ASSERTING TX LINE AFTER RISING EDGE OF SELECT LINE		2 CORE SPI CLOCK PERIODS +3 NSEC	MIXED
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	30		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER FALLING EDGE OF SPI CLOCK	10		NSEC
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD LOW AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	1		MSPI CLOCK PERIOD

**TIMING DIAGRAM, SLAVE MODE, SPO=1, SPH=0**



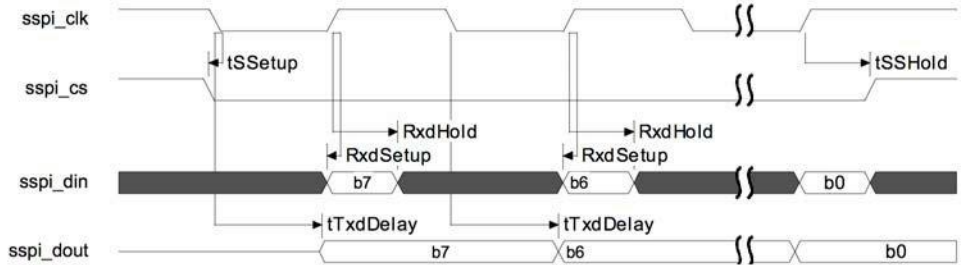
PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSetup	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST FALLING EDGE OF SPI CLOCK	4 CORE SPI CLOCK PERIODS +68 NSEC		MIXED
TTxDelay	DELAY IN SLAVE ASSERTING TX LINE AFTER FALLING EDGE OF SPI CLOCK, OR THE FIRST BIT AFTER FALLING EDGE OF SELECT LINE		4 CORE SPI CLOCK PERIODS +68 NSEC	MIXED
TRxDSetup	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	15		NSEC
TRxDHold	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	3 CORE SPI CLOCK PERIODS +14 NSEC		MIXED
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	3 CORE SPI CLOCK PERIODS +14 NSEC		MSPI CLOCK PERIOD

**H-4. MOTOROLA SPI, CLOCK POLARITY SPO = 1, CLOCK PHASE SPH = 1  
 TIMING DIAGRAM, MASTER MODE, SPO=1, SPH=1**



PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSetup	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST FALLING EDGE OF SPI CLOCK	1.5		MSPI CLOCK PERIOD
TTxDelay	DELAY IN MASTER ASSERTING TX LINE AFTER FALLING EDGE OF SPI CLOCK		0	NSEC
TRxDSetup	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	30		NSEC
TRxDHold	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	10		NSEC
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD LOW AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	0.5		MSPI CLOCK PERIOD

**TIMING DIAGRAM, SLAVE MODE, SPO=1, SPH=1**

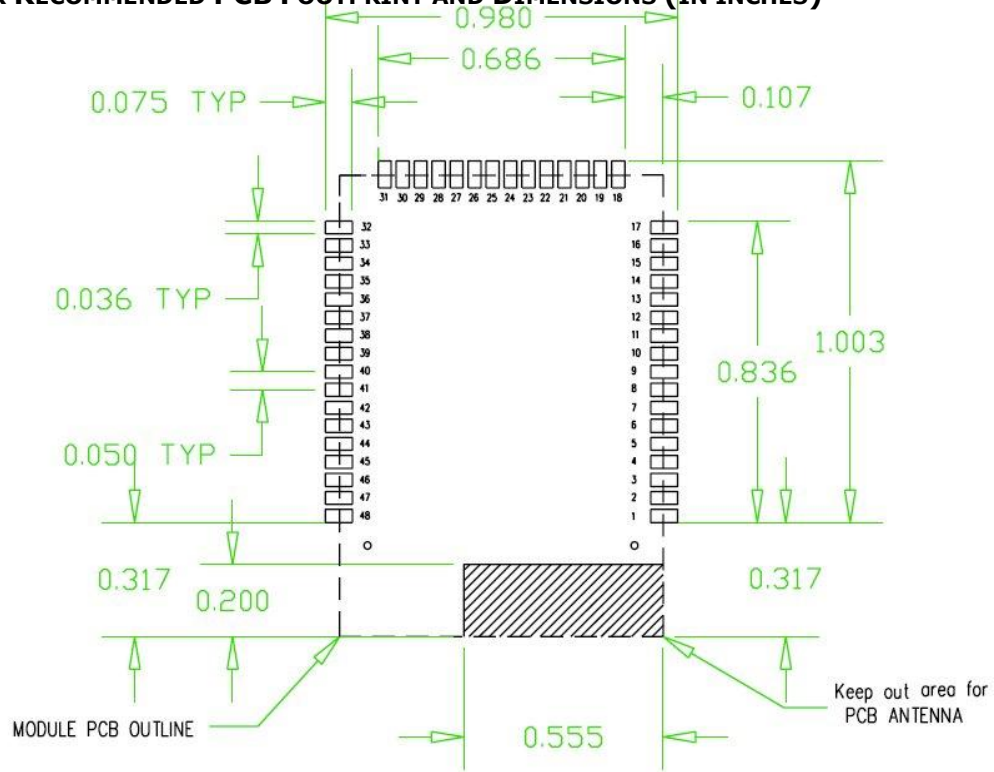


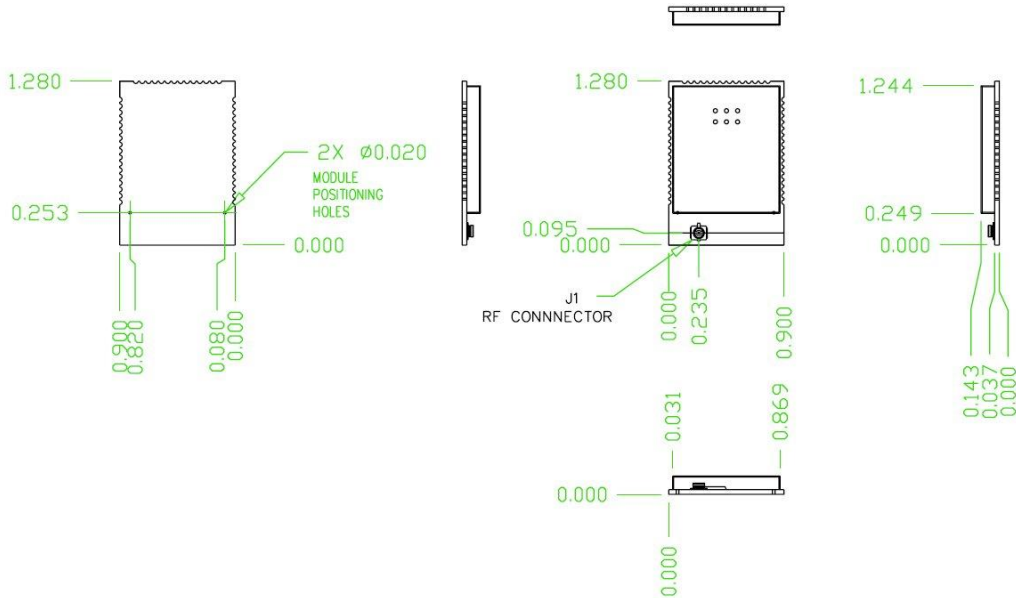
PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
TSSSETUP	MINIMUM TIME BETWEEN FALLING EDGE OF SELECT LINE AND FIRST FALLING EDGE OF SPI CLOCK	4 CORE SPI CLOCK PERIODS +68 NSEC		MIXED
TTXDDELAY	DELAY IN SLAVE ASSERTING TX LINE AFTER FALLING EDGE OF SPI CLOCK, OR THE FIRST BIT AFTER FALLING EDGE OF SELECT LINE		4 CORE SPI CLOCK PERIODS +68 NSEC	MIXED
TRXDSETUP	TIME BEFORE RISING EDGE OF SPI CLOCK BY WHICH RECEIVED DATA MUST BE READY	15		NSEC
TRXDHOLD	TIME FOR WHICH RECEIVED DATA MUST BE STABLE AFTER RISING EDGE OF SPI CLOCK	3 CORE SPI CLOCK PERIODS +14 NSEC		MIXED
TSSHOLD	TIME FOR WHICH THE SELECT LINE WILL BE HELD AFTER THE SAMPLING EDGE FOR THE FINAL BIT TO BE TRANSFERRED	3 CORE SPI CLOCK PERIODS +14 NSEC		MSPI CLOCK PERIOD

**PACKAGE AND LAYOUT GUIDELINES**

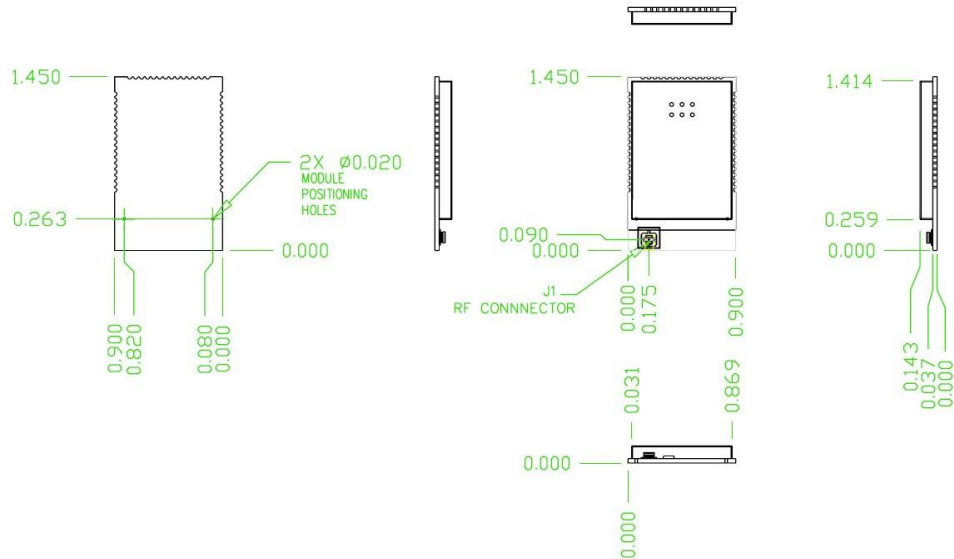
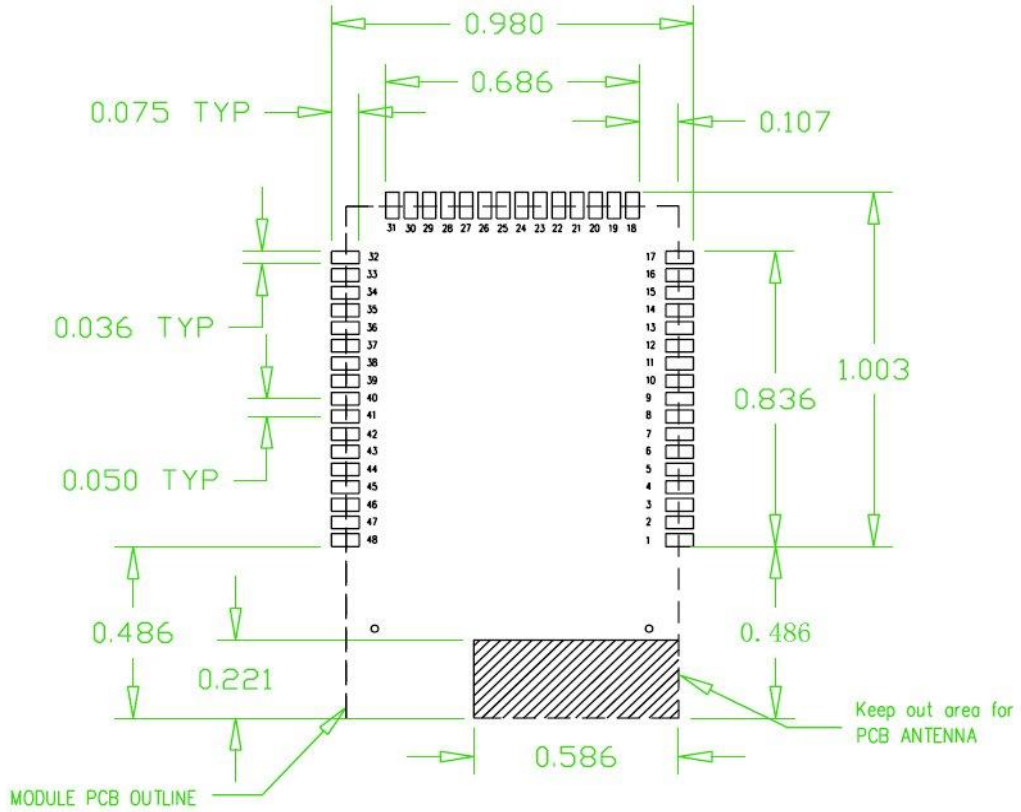
DIMENSIONS ARE IN INCHES

**J-1. WL11-IX RECOMMENDED PCB FOOTPRINT AND DIMENSIONS (IN INCHES)**

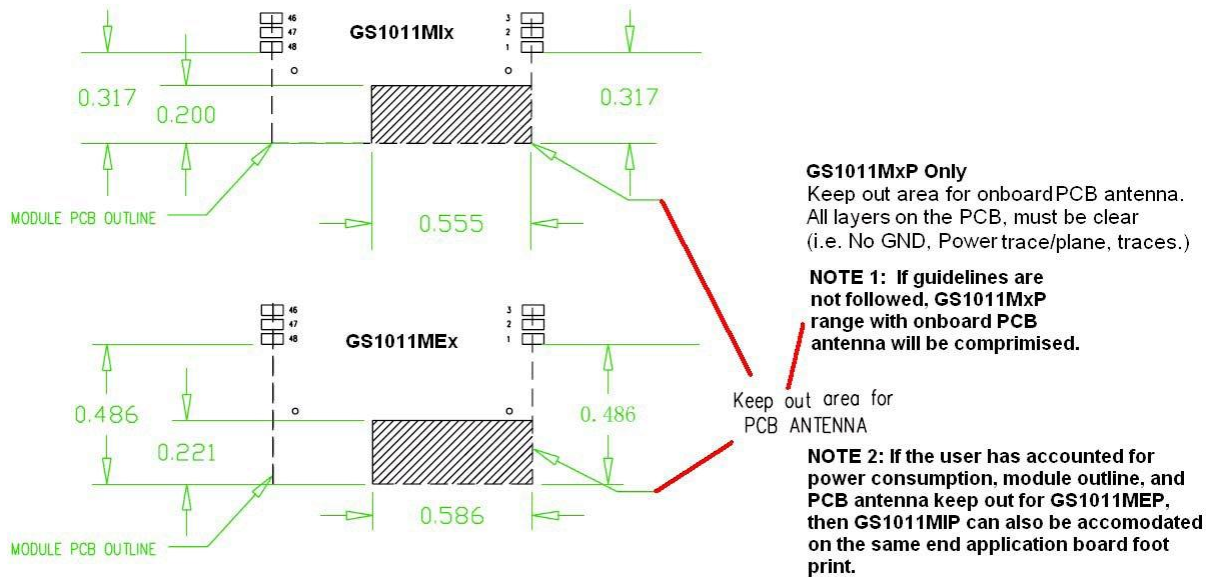




**J-2. WL11-EX RECOMMENDED PCB FOOTPRINT AND DIMENSIONS (IN INCHES)**



**J-3. WL11-XX LAYOUT GUIDELINES (IN INCHES)**



**IN ADDITION TO THE GUIDELINES IN THE PREVIOUS FIGURES, NOTE THE FOLLOWING SUGGESTIONS:**

**WL11-Ex AND WL11-Ix**

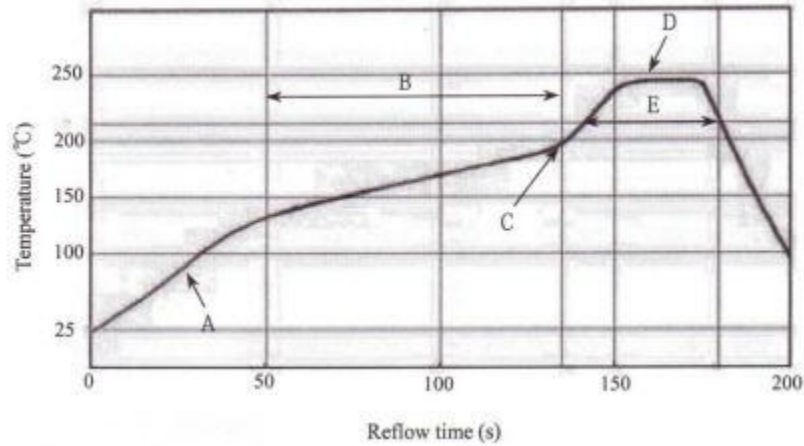
- EXTERNAL BYPASS CAPACITORS FOR ALL MODULE SUPPLIES SHOULD BE AS CLOSE AS POSSIBLE TO THE MODULE PINS.
- NEVER PLACE THE ANTENNA VERY CLOSE TO METALLIC OBJECTS
- THE EXTERNAL DIPOLE ANTENNAS NEED A REASONABLE GROUND PLANE AREA FOR ANTENNA EFFICIENCY

**WL11-xP ONBOARD PCB ANTENNA SPECIFIC**

- THE PCB ANTENNA KEEP OUT AREA, AS SHOWN IN J-2, MUST BE ADHERED TO (I.E. NO GROUND, POWER TRACE/PLANE, TRACES; ALL LAYERS OF PCB, IN THE KEEP OUT AREA, MUST BE CLEAR), OR THE OVER THE AIR RANGE OF THE WF11MXP WILL BE COMPROMISED.
- DO NOT USE A METALLIC OR METALIZED PLASTIC FOR THE END PRODUCT ENCLOSURE
- KEEP PLASTIC ENCLOSURE 1 CM MIN HEIGHT ABOVE THE WF11-MXP PCB ANTENNA WHILE MAINTAINING THE KEEP OUT AREA, AS SHOWN IN FIGURE J-3.

**SURFACE MOUNT ASSEMBLY**

THE REFLOW PROFILE<sup>1</sup> IS SHOWN BELOW. RECOMMENDED REFLOW PARAMETERS ARE SUMMARIZED IN THE TABLE BELOW.



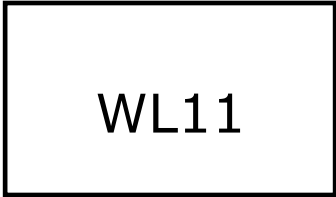
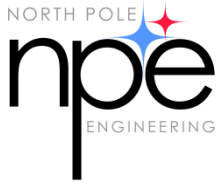
**REFLOW PROFILE FIGURE**

**REFLOW PARAMETERS**

PROFILE FEATURE PREHEAT	NOTES	
Temperature Ramp up rate for (A)	2	2 - 4 °C/s
Pre-heat time (b)	3	60 - 120 seconds
Pre-heat ending temperature (C)	4	180 - 200 °C
HEATING <sup>5</sup>		
Peak Temperature range (D)		230 - 240 °C
Melting time that is the time over 220 °C (E)		20 to 40 seconds

Notes:

1. Perform adequate test in advance as the reflow temperature profile will vary accordingly to the conditions of the parts and boards, and the specifications of the reflow furnace.
2. Be careful about rapid temperature rise in preheat zone as it may cause excessive slumping of the solder paste.
3. If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will generate in clusters at a time.
4. If the temperature is too low, non-melting tends to be caused in the area with large heat capacity after reflow.
5. Be careful about sudden rise in temperature as it may worsen the slump of solder paste.
6. Be careful about slow cooling as it may cause the positional shift of parts and decline in joining strength at times.



FCC ID

The WiFi-IT has been FCC/IC certified. The modules are RoHS and CE compliant and meet EU /R&TTE Directive for Radio Spectrum.

	<b>WL11-IP</b>	<b>WL11-EP</b>	<b>WL11-IE</b>	<b>WL11-EE</b>
FCC ID	YOPGS1011MIP	YOPGS1011MEP	YOPGS1011MIE	YOPGS1011MEE

**REGULATORY NOTES**

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: To assure continued compliance, (example - use only shielded interface cables when connecting to computer or peripheral devices). Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

**FCC & IC Radiation Exposure Statement:**

This equipment complies with FCC & IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter. This device is intended only for OEM integrators under the following conditions:

- 1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
- 2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

**IMPORTANT NOTE:** In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC & IC authorizations are no longer considered valid and the FCC & IC IDs cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining separate FCC & IC authorizations.

#### **END PRODUCT LABELING**

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users (for example access points, routers, wireless ADSL modems, and similar equipment). The final end product must be labeled in a visible area with the corresponding FCC ID number.

#### **IC CERTIFICATION — CANADA**

The labeling requirements for Industry Canada are similar to those of the FCC. A visible label on the outside of the final product must display the IC labeling. The user is responsible for the end product to comply with IC ICES-003 (Unintentional radiators)

#### **MANUAL INFORMATION THAT MUST BE INCLUDED**

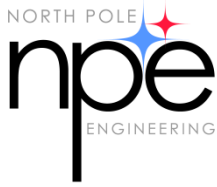
The user's manual for end users must include the following information in a prominent location.

**IMPORTANT NOTE:** To comply with FCC & IC RF exposure compliance requirements, the antenna used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter.

#### **Other notes:**

GainSpan modules have been built or under development for near body exposure applications. The 20cm statement is a standard note because absorption rate testing (commonly known as SAR or Specific absorption rate) is not modularly transferable for FCC/IC. Thus, if a radio is being used against the body, the end user is still responsible to test for regulatory near body exposure testing (for USA, please refer to the following):

- FCC Part 1.1037
- FCC Part 2.1091 Mobile Devices
- FCC Part 2.1093 Portable Devices
- FCC Part 15.247 (b) (4)



**ORDERING INFORMATION**

The WiFi-IT! modules can be ordered with or without the WiFi-Basic Run Time Engine firmware loaded in either of two antenna configurations.

Part numbers with the 'R' suffix include the WiFi-Basic Run-Time Engine (RTE) firmware.

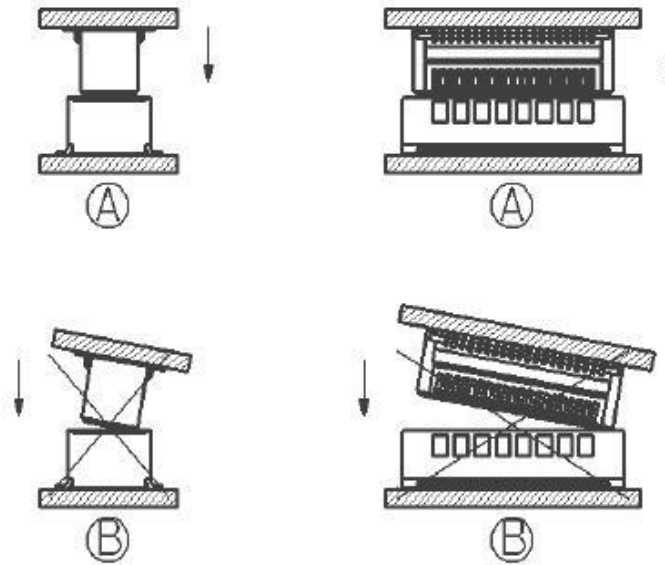
Part numbers with the 'C' suffix include the WiFi-Basic Run-Time Engine (RTE) firmware and are mounted on a carrier board for use with the NPE Evaluation & Development Kits; EDK and EDK+.

Part Number	Description
WL11-IPR	Internal Power Amplifier / PCB antenna / WiFi-Basic RTE.
WL11-EPR	External Power Amplifier / PCB antenna / WiFi-Basic RTE.
WL11-IER	Internal Power Amplifier / External antenna / WiFi-Basic RTE.
WL11-EER	External Power Amplifier / External antenna / WiFi-Basic RTE.
WL11-IP	Internal Power Amplifier / PCB antenna / AT-command Set
WL11-EP	External Power Amplifier / PCB antenna / AT-command Set
WL11-IE	Internal Power Amplifier / External antenna / AT-command Set
WL11-EE	External Power Amplifier / External antenna / AT-command Set
WL11-IPC	Internal Power Amplifier / PCB antenna / WiFi-Basic RTE / Carrier Board
WL11-EPC	External Power Amplifier / PCB antenna / WiFi-Basic RTE / Carrier Board
WL11-IEC	Internal Power Amplifier / External antenna / WiFi-Basic RTE / Carrier Board
WL11-EEC	External Power Amplifier / External antenna / WiFi-Basic RTE / Carrier Board

Order directly from the NPE website at [www.npe-inc.com](http://www.npe-inc.com) or contact NPE Sales at 612-305-0440 x3 for volume pricing.

**WiFi-IT CONNECTOR MATING**

When ordering modules for use with the EDK or EDK+ (-C suffix), please follow these instructions when attaching the module to the EDK development card.



**ENGINEER’S DESIGN CHECKLIST**

This design checklist should be reviewed before committing a design to PCB fabrication. The checklist contains items that affect performance and/or operation of the WiFi-IT! module.

<b>SCHEMATIC DESIGN CHECKLIST</b>		
<b>ITEM</b>	<b>DESCRIPTION</b>	<b>Y/N</b>
1	Verify WL11 pin numbers on schematic.	
2	Have all ground (GND) connections, pins 1,17,32 and 48, been connected to the same ground plane?	
3	If ALARM1 is used it must be driven from a signal on the VBAT voltage plane.	
4	If ALARM2 is used it must be driven from a signal on the VBAT voltage plane.	
5	EXT_RESETh is an output during power up. After module reset is complete this pin is an input. If EXT_RESETh is used to reset external devices, has it been pulled high to VDD_IO through a resistor?	
6	GPIO27 is used to place the module into boot loader mode. This allows code to be loaded into the WL11 processor. Can GPIO27 be driven to VDD_IO during module power on to support boot loader mode?	
7	GPIO25 is used by WiFi-Basic to enter override mode, where debugging operations can take place. If using WiFi-Basic, can GPIO25 be driven to VDD_IO to enter override mode?	
8	GPIO28 and GPIO29 are used to configure the JTAG interface during module reset. These signals should not be driven from an external device, if JTAG debugging is to be supported. If using JTAG, are GPIO28 and GPIO29 unconnected or configured as outputs only?	
9	If I2C interface is used, have pins 25 and 26 (I2C_CLK and I2C_DATA) been pulled up to VDD_IO through 2K Ohm pull-ups?	

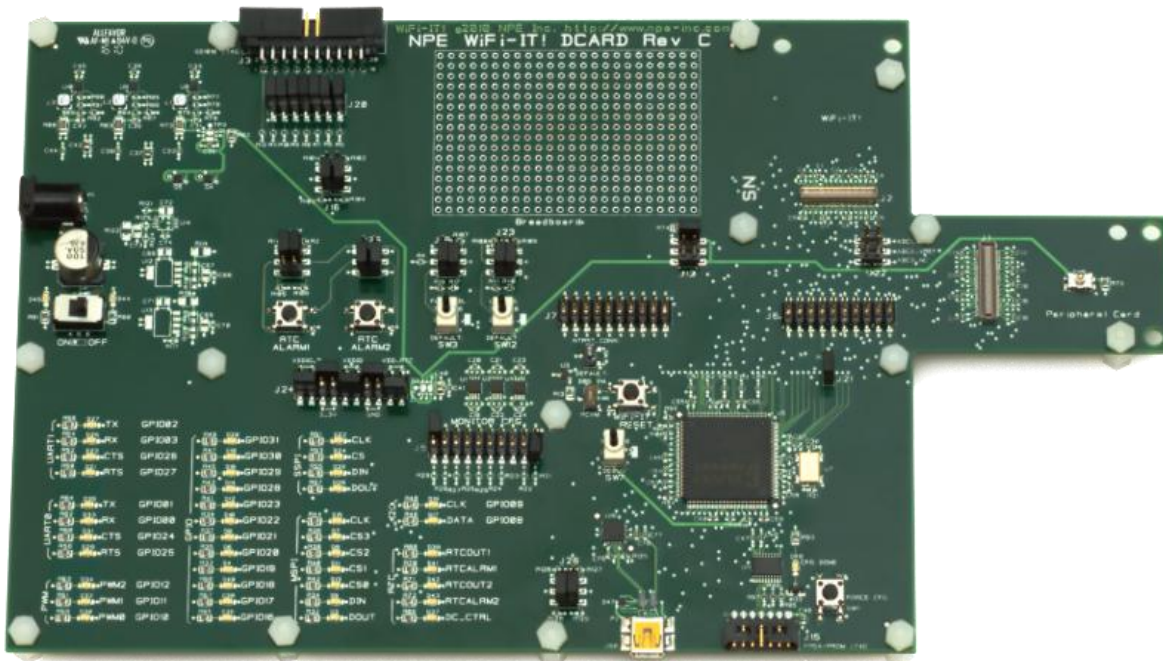
<b>SCHEMATIC DESIGN CHECKLIST</b>		
<b>ITEM</b>	<b>DESCRIPTION</b>	<b>Y/N</b>
10	GPIO30 and GPIO31 are high-drive (up to 20 mA each) output ports. Have devices requiring more than 4 mA drive been connected to GPIO30 and/or GPIO31?	
11	ADC inputs are limited to 1.8v input, when referenced to VOUT_1V8. Have any analog signals, measured by the ADC, been limited to 1.8v?	

<b>PCB DESIGN CHECKLIST</b>		
<b>ITEM</b>	<b>DESCRIPTION</b>	<b>Y/N</b>
1	VDD traces and vias to the WiFi-IT! connector are sized to carry 200 mA per connector pin. Two vias per WiFi-IT! connector VDD pin may be necessary.	
2	External bypass capacitors for all module voltage supplies should be as close as possible to the associated module pins.	
3	When using a module with a PCB antenna (WL11-IPx / WL11-EPx) the antenna portion of the module should be unobstructed. E.g. The PCB antenna hangs off the edge of the base board PCB or the base board PCB is cut back. A minimum of .2" of clearance is available to the PCB antenna.	
4	No metallic objects are places close to the PCB antenna.	
5	It is recommended not to run traces underneath the module especially near the RF shield mounting holes, as they are grounded.	

## WiFi-IT! EDK & EDK+

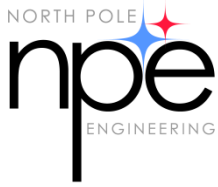
The EDK and EDK+ Evaluation and Development Systems allow you to evaluate and develop embedded systems using the WiFi-IT! module. Both the EDK and EDK+ include WiFi-Basic which allows you to run your programs directly on the WiFi-IT module.

The EDK platform board (DCard) provides easy access to all of the WiFi-IT! interfaces and visual indication of interface signaling, thereby reducing the need for an oscilloscope and/or logic analyzer. The EDK supports access to the WiFi-IT! UART0 port through the onboard USB. The USB interface can be used to download code, setup configuration information, loading code and debug programs.



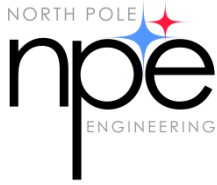
The EDK contains two WiFi-IT! modules, the EDK platform board (Dcard), a pre-configured Access Point and the complete Integrated Development Environment, for writing, debugging and testing application code that runs directly on the WiFi-IT! module.

A full description of the EDK development system is available from North Pole Engineering, Inc. at our website – [www.npe-inc.com](http://www.npe-inc.com).



**REVISION HISTORY**

VERSION	DATE	DESCRIPTION
0.5	12/15/2010	First release.
0.6	03/31/2011	Corrected signal descriptions. Added standard power configuration design examples. Updated power supply example.
1.0	05/31/2011	Added table of contents. Updated missing specifications.
1.1	09/01/2011	Updated designers checklists. Removed Alarm1 alternate function as it was incorrect. Corrected part numbers for ordering.



WiFi-IT!™  
WLAN Module

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WL11

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